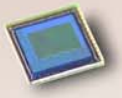
OmniVision



datasheet

PRODUCT SPECIFICATION

1/4" color CMOS UXGA (2 megapixel) image sensor
with OmniPixel3-HS™ technology

OV2643

color CMOS UXGA (2 megapixel) image sensor with OmniPixel3-HS™ technology

datasheet (CSP3)
PRODUCT SPECIFICATION

version 2.0
august 2010

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- cellular phones
- toys
- PC multimedia
- digital still cameras

ordering information

- **OV02643-A42A** (color, lead-free)
  42-pin CSP3

features

- ultra low power and low cost
- automatic image control functions: automatic exposure/gain control (AEC/AGC), automatic white balance (AWB), automatic band filter (ABF), and automatic black level calibration (ABLC)
- programmable controls for frame rate, AEC/AGC 16-zone size/position/weight control, mirror and flip, and windowing
- image quality controls: color saturation, hue, gamma, sharpness (edge enhancement), lens correction, defective pixel canceling, and noise canceling
- support for output formats: RAW RGB, RGB565/555, YUV422, YCbCr422 and GBR422
- support for images sizes: UXGA, SVGA, and 720p
- support for video operations
- support for horizontal and vertical sub-sampling, binning
- standard serial SCCB interface
- digital video port (DVP) parallel output interface
- on-chip phase lock loop (PLL)
- programmable I/O drive capability
- support for black sun cancellation
- built-in regulator for DVDD
- suitable for module size of 6.5 mm x 6.5 mm

key specifications

- **active array size:** 1624 x 1212
- **power supply:**
  core: 1.5VDC ± 5%
  analog: 2.6 ~ 3.0V
  I/O: 1.7 ~ 3.0V
- **power requirements:**
  active: 150 mW
  standby: 30 µA
- **temperature range:**
  operating: -20°C to 70°C (see **table 8-2**)
  stable image: 0°C to 50°C (see **table 8-2**)
- **output formats (8-bit):** YUV422 / YCbCr422, GBR422, RGB565/555, 8-/10-bit raw RGB data
- **lens size:** 1/4"
- **lens chief ray angle:** 25° non-linear (see **figure 10-2**)
- **input clock frequency:** 6 ~ 27 and 54 MHz
- **S/N ratio:** 39 dB
- **dynamic range:** 66 dB
- **maximum image transfer rate:**
  UXGA (1600x1200): 15 fps
  SVGA (800x600): 30 fps
  720p (1280x720): 30 fps
- **sensitivity:** 1250 mV/Lux-sec
- **shutter:** rolling shutter
- **scan mode:** progressive
- **maximum exposure interval:** 1227 x t_{ROW}
- **gamma correction:** programmable
- **pixel size:** 2.2 µm x 2.2 µm
- **well capacity:** 11 Ke^-
- **dark current:** 8 mV/s @ 50ºC
- **fixed pattern noise (FPN):** <1% of $V_{PEAK-TO-PEAK}$
- **image area:** 3590 µm x 2710 µm
- **package dimensions:** 5035 µm x 4635 µm

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV2643 image sensor. The package information is shown in section 9.

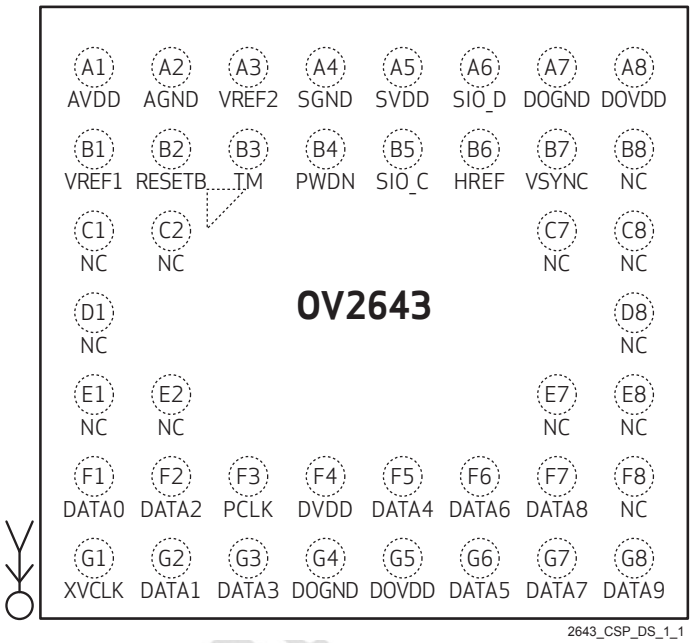
table 1-1 signal descriptions (sheet 1 of 2)

pin number	signal name	pin type	description	default I/O status
A1	AVDD	power	power for analog circuit	
A2	AGND	ground	ground for analog circuit	
A3	VREF2	reference	internal analog reference	
A4	SGND	ground	ground for sensor array	
A5	SVDD	power	power for sensor array	
A6	SIO_D	I/O	SCCB data	
A7	DOGND	ground	ground for digital core and I/O circuit	
A8	DOVDD	power	power for I/O circuit	
B1	VREF1	reference	internal analog reference	
B2	RESETB	input	reset (active low with internal pull-up resistor)	
B3	TM	input	test mode (active high with internal pull-down resistor)	
B4	PWDN	input	power down (active high with internal pull-down resistor)	
B5	SIO_C	input	SCCB input clock	
B6	HREF	I/O	horizontal reference output	input
B7	VSYNC	I/O	vertical sync output	input
B8	NC	–	no connect	
C1	NC	–	no connect	
C2	NC	–	no connect	
C7	NC	–	no connect	
C8	NC	–	no connect	
D1	NC	–	no connect	
D8	NC	–	no connect	
E1	NC	–	no connect	

table 1-1 signal descriptions (sheet 2 of 2)

pin number	signal name	pin type	description	default I/O status
E2	NC	–	no connect	
E7	NC	–	no connect	
E8	NC	–	no connect	
F1	DATA0	I/O	digital video port bit[0]	input
F2	DATA2	I/O	digital video port bit[2]	input
F3	PCLK	I/O	pixel clock output	input
F4	DVDD	reference	power for digital core	
F5	DATA4	I/O	digital video port bit[4]	input
F6	DATA6	I/O	digital video port bit[6]	input
F7	DATA8	I/O	digital video port bit[8]	input
F8	NC	–	no connect	
G1	XVCLK	input	system input clock	
G2	DATA1	I/O	digital video port bit[1]	input
G3	DATA3	I/O	digital video port bit[3]	input
G4	DOGND	ground	ground for digital core and I/O circuit	
G5	DOVDD	power	power for I/O circuit	
G6	DATA5	I/O	digital video port bit[5]	input
G7	DATA7	I/O	digital video port bit[7]	input
G8	DATA9	I/O	digital video port bit[9]	input

figure 1-1 pin diagram



2643_CSP_DS_1_1

2 system level description

2.1 overview

The OV2643 (color) image sensor is a low voltage, high-performance 1/4-inch 2.0 megapixel CMOS image sensor that provides the full functionality of a single chip UXGA (1600x1200) camera using OmniPixel3-HS™ technology in a small footprint package. It provides full-frame, sub-sampled, windowed or cropped 8-bit/10-bit images in various formats via the control of the Serial Camera Control Bus (SCCB) interface.

The OV2643 has an image array capable of operating at up to 15 frames per second (fps) in UXGA resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control, defective pixel canceling, noise canceling, etc., are programmable through the SCCB interface. In addition, Omnivision image sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

2.2 architecture

The OV2643 sensor core generates streaming pixel data at a constant frame rate, indicated by HREF and VSYNC. **figure 2-1** shows the functional block diagram of the OV2643 image sensor. **figure 2-2** shows an example application using an OV2643 sensor.

The timing generator outputs signals to access the rows of the image array, precharging and sampling the rows of array in series. In the time between pre-charging and sampling a row, the charge in the pixels decreases with the time exposed to the incident light. This is known as exposure time.

The exposure time is controlled by adjusting the time interval between precharging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs 10-bit data for each pixel in the array.

figure 2-1 OV2643 block diagram

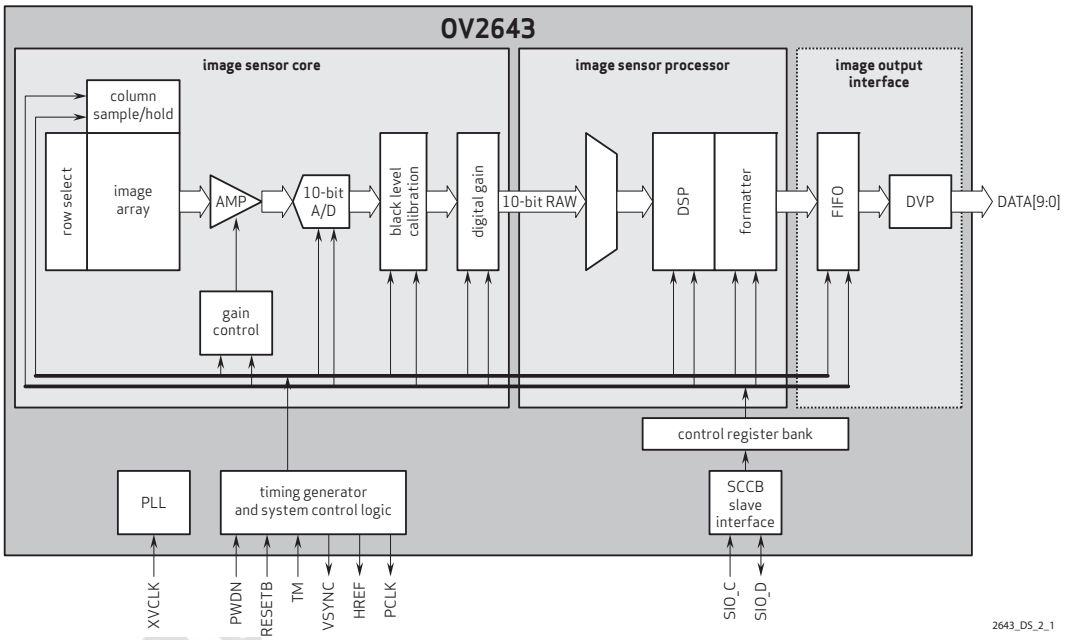
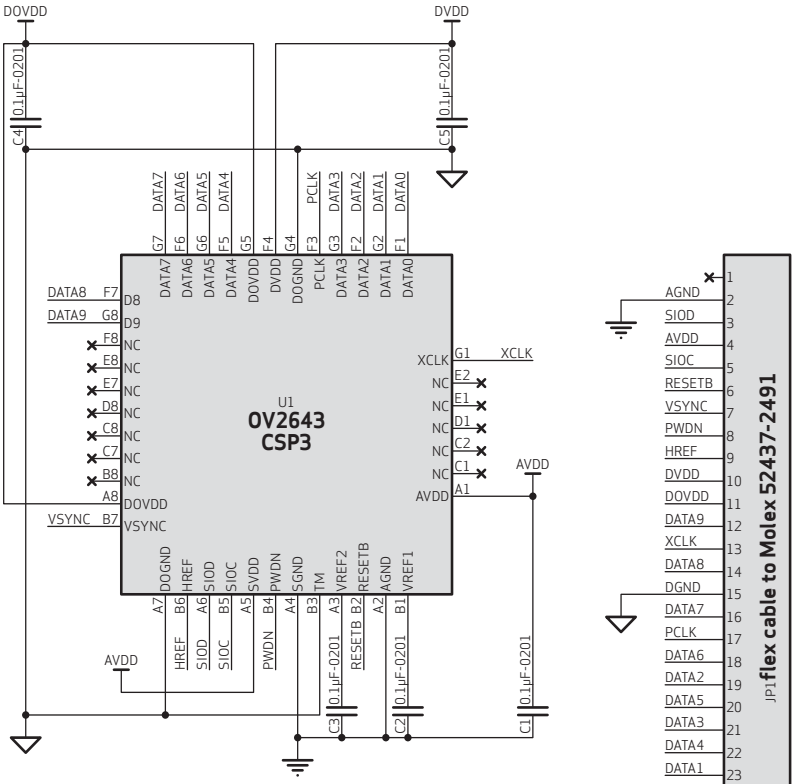


figure 2-2 camera module reference design schematic



note 1 RESETB should be connected to DOVDD outside of module if unused.

note 2 AVDD is the power supply for sensor analog circuit. Typical voltage is 2.8 V (range = 2.6 - 3.0 V). Sharing with other devices is not recommended.

note 3 DVDD is 1.5 V ±5% of sensor digital power.

note 4 DOVDD is the power supply for IO device and the internal regulator which generates 1.5 V supply for digital core. The typical voltage is 1.8 V (range = 1.70 - 3.0 V).

note 5 sensor AGND and DGND should be separated and connected to a single point outside the module (do not connect inside the module).

note 6 decoupling capacitors should be close to the related sensor pins.

note 7 D[9:0] (D9:MSB, D0:LSB) is sensor 10-bit raw RGB output. D[9:2] (D9:MSB, D2:LSB) is 8-bit output.

2643_CSP_DS_2_2

2.3 I/O control

The OV2643 I/O pad direction and driving capability can be easily adjusted. **table 2-1** lists the driving capability and direction control registers of the I/O pins.

table 2-1 driving capability and direction control for I/O pads

function	register	description
output drive capability control	0xC3	Bit[7:6]: output drive capability 00: 1x 01: 2x 10: 3x 11: 4x
DATA[9:0] I/O control	{0xC3[1:0], 0xC4[7:0]}	input/output selection for the DATA[9:0] pins 0: input 1: output
VSYNC I/O control	0xC3	Bit[3]: input/output selection for the VSYNC pin 0: input 1: output
HREF I/O control	0xC3	Bit[4]: input/output selection for the HREF pin 0: input 1: output
PCLK I/O control	0xC3	Bit[2]: input/output selection for the PCLK pin 0: input 1: output

2.4 format and frame rate

table 2-2 format and frame rate

format	resolution	frame rate	scaling method	parallel port data rate (RAW/YUV)
UXGA	1600x1200	15 fps	full	36/72 MHz
SVGA	800x600	30 fps	down sampling	36/72 MHz
CIF	400x300	30 fps	down sampling	18/36 MHz
QCIF	200x150	30 fps	down sampling	9/18 MHz
720p	1280x720	30 fps	down sampling	36/72 MHz

2.5 power up sequence

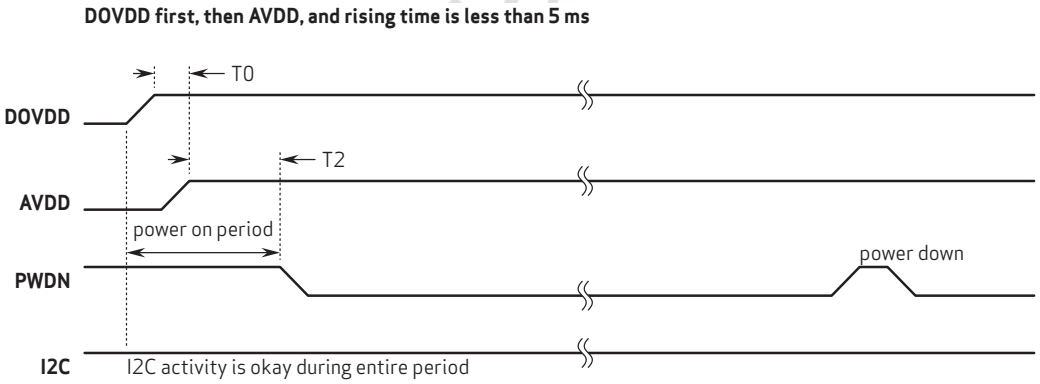
Based on the system power configuration (1.8V or 2.8V for I/O power, using external DVDD or internal DVDD, requiring access to the I2C during power up period or not), the power up sequence will differ. If 1.8V is used for I/O power, using the internal DVDD is preferred.

2.5.1 power up with internal DVDD

For powering up with the internal DVDD and I2C access during the power ON period, the following conditions must occur:

1. if DOVDD and AVDD are turned ON at the same time, make sure DOVDD becomes stable before AVDD becomes stable
2. PWDN is active high with an asynchronized design (does not need clock)
3. PWDN must go high if I2C is accessed during the power up period
4. for PWDN to go low, power must first become stable (AVDD to PWDN ≥ 1 ms)
5. RESETB is active low with an asynchronized design
6. state of RESETB does not matter during power up period once DOVDD is up

figure 2-3 power up timing with internal DVDD



note T0 ≥ 0 ms: delay from DOVDD stable to AVDD stable
T2 ≥ 1 ms: delay from AVDD stable to sensor power up stable

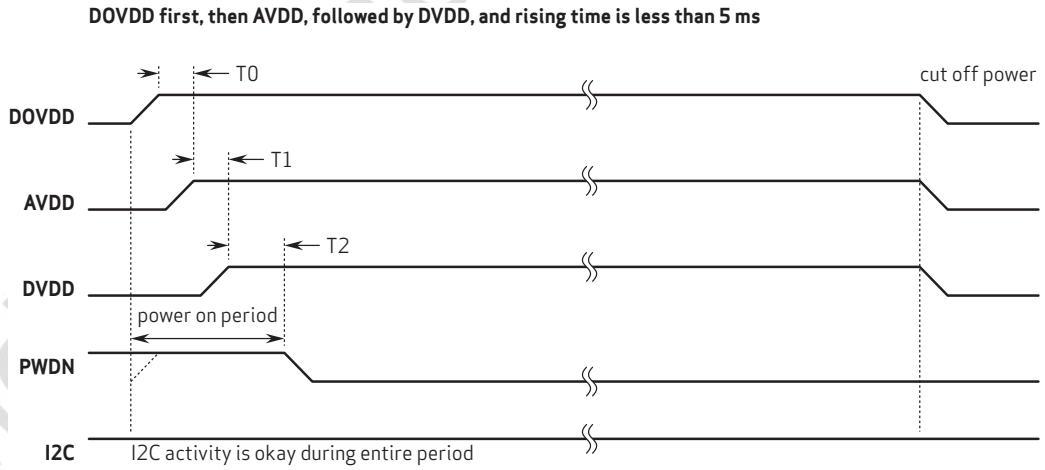
2643_DS_2_3

2.5.2 power up with external DVDD source

For powering up with an external DVDD source and I2C access during the power ON period, the following conditions must occur:

1. if DOVDD and AVDD are turned ON at the same time, make sure DOVDD becomes stable before AVDD becomes stable
2. if AVDD and DVDD are turned ON at the same time, make sure AVDD becomes stable before DVDD becomes stable
3. PWDN is active high with an asynchronized design (does not need clock)
4. for PWDN to go low, power must first become stable (DVDD to PWDN ≥ 1 ms)
5. RESETB is active low with an asynchronized design
6. state of RESETB does not matter during power up period once DOVDD is up

figure 2-4 power up timing with external DVDD source



note T0 ≥ 0 ms: delay from DOVDD stable to AVDD stable
T1 ≥ 0 ms: delay from AVDD stable to DVDD stable
T2 ≥ 1 ms: delay from DVDD stable to sensor power up stable

2643_DS_2_4

2.6 reset

The OV2643 sensor includes a RESETB pin that forces a complete hardware reset when it is pulled low (GND). The OV2643 clears all registers and resets them to their default values when a hardware reset occurs. A reset can also be initiated through the SCCB interface by setting register 0x12[7] to high.

The whole chip will be reset during power up. Manually applying a hard reset upon power up is recommended even though the on-chip power up reset is included. The hard reset is active low with an asynchronized design. The reset pulse width should be greater than or equal to 1 ms.

2.7 standby and sleep

Two suspend modes are available for the OV2643:

- hardware standby
- SCCB software sleep

To initiate hardware standby mode, PWDN pin must be tied to high (see **figure 2-5**).

figure 2-5 power down/ wake up sequence

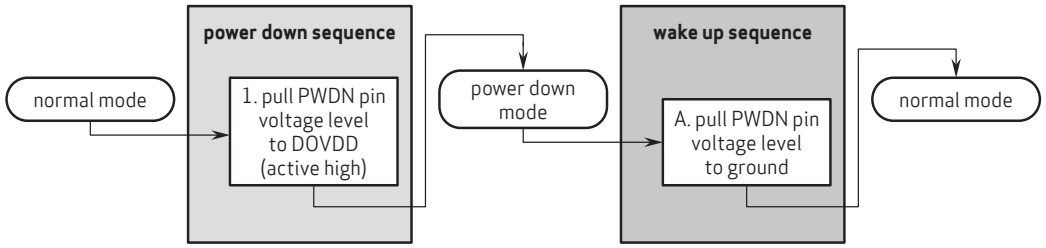
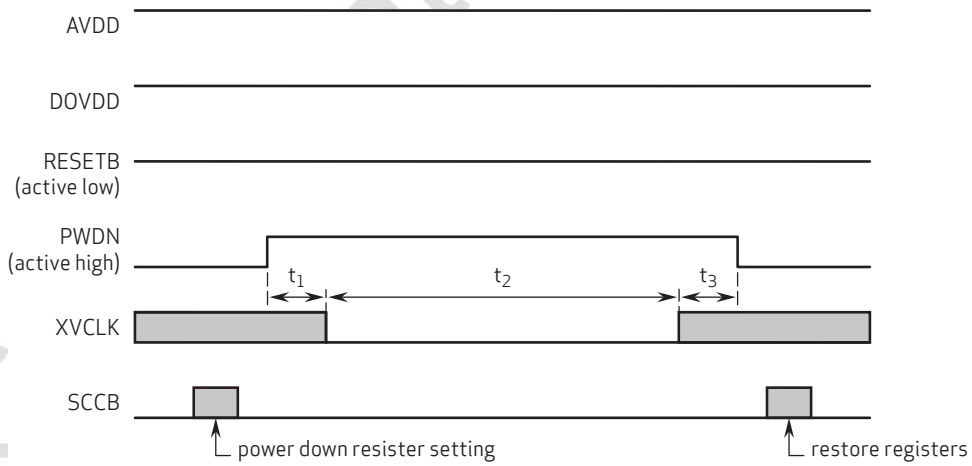


figure 2-6 power down timing diagram



note t_1: XVCLK should keep more than 0.1ms after PWDN is pulled high
t_2: power down period should last more than 1 frame period
t_3: XVCLK should come more than 0.1ms before PWDN is pulled low

2643_DS_2_6

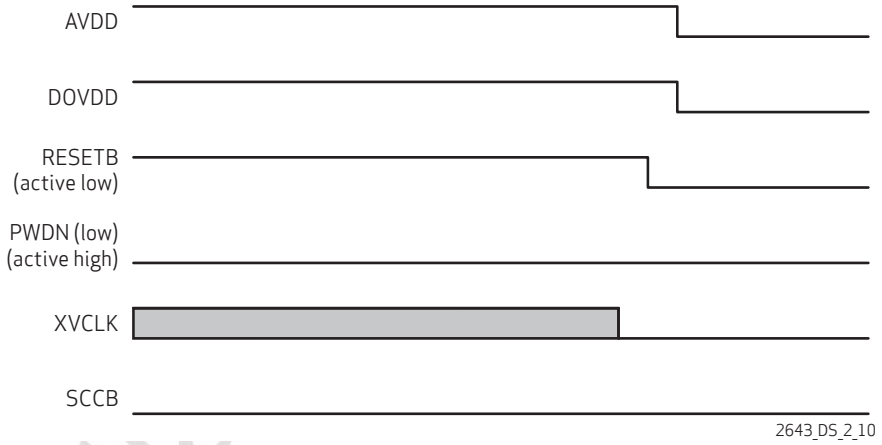
When this occurs, the OV2643 internal device clock is halted and all internal counters are reset and registers are maintained.

Executing a software power-down through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in standby mode.

2.8 power OFF sequence

Powering off timing for the OV2643 sensor is described in **figure 2-7**.

figure 2-7 power OFF timing diagram



2.9 system clock control

The OV2643 PLL allows for an input clock frequency ranging from 6~27 MHz. The PLL can be bypassed by setting register 0x10[6] to 1.

2.10 SCCB interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the OmniVision Technologies Serial Camera Control Bus (SCCB) Specification for detailed usage of the serial control port.

3 block level description

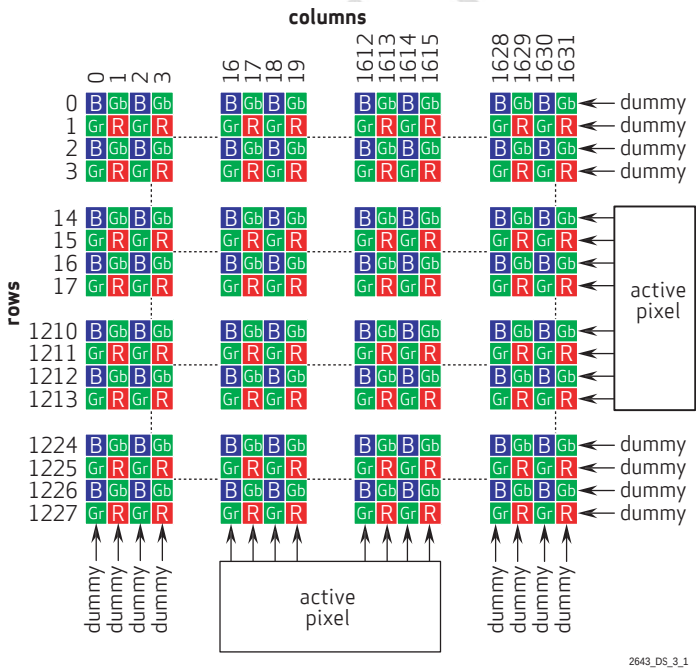
3.1 pixel array structure

The OV2643 sensor has an image array of 1632 columns by 1228 rows (2,004,096 pixels). figure 3-1 shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 2,004,096 pixels, 1,920,000 (1600x1200) are active pixels and can be output. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

figure 3-1 sensor array region color filter layout



4 image sensor core digital functions

4.1 mirror and flip

The OV2643 provides Mirror and Flip read-out modes, which respectively reverse the sensor data read-out order horizontally and vertically (see **figure 4-1**). In mirror, since the Bayer order changes from BGBG... to GBGB..., the OV2643 usually automatically delays the read-out sequence by one pixel. In flip, the OV2643 does not need additional settings because the ISP block will auto-detect whether the pixel is in the red line or blue line and make necessary adjustments.

figure 4-1 mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

2643_DS_4_1

table 4-1 mirror and flip function control

function	register	description
mirror	0x12	Bit[5]: mirror ON/OFF select 0: mirror OFF 1: mirror ON
flip	0x12	Bit[4]: flip ON/OFF select 0: flip OFF 1: flip ON

4.2 image windowing

An image windowing area is defined by four parameters, horizontal start (HS), horizontal width (HW), vertical start (VS), and vertical height (VH). By properly setting the parameters, any portion within the sensor array size can be cropped as a visible area. This windowing is achieved by simply masking the pixels outside the window; thus, it will not affect original timings. It will also not conflict with the flip and mirror functions.

figure 4-2 image windowing

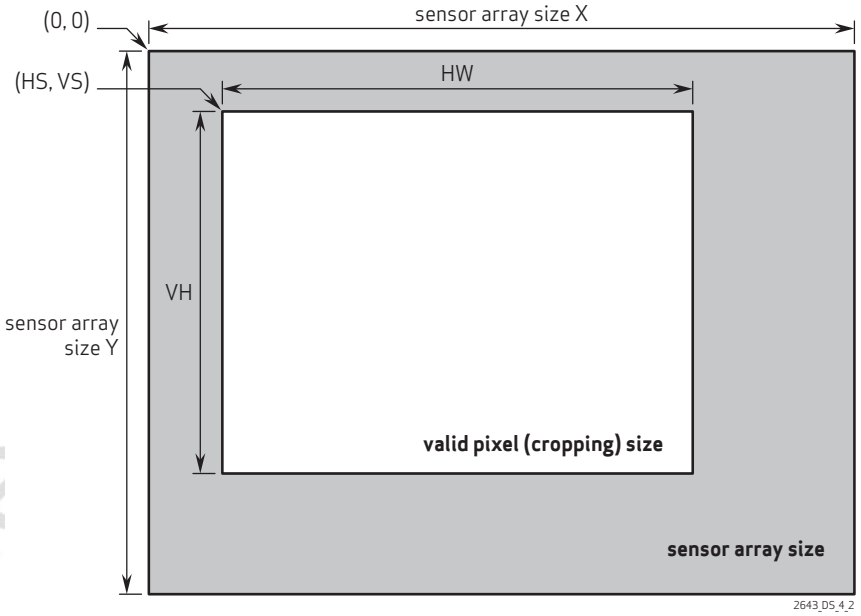


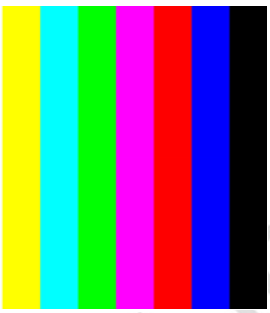
table 4-2 image windowing control functions

function	register	description
horizontal start	[0x20, 0x21]	HS[15:8] = 0x20 HS[7:0] = 0x21
vertical start	[0x22, 0x23]	VS[15:8] = 0x22 VS[7:0] = 0x23
horizontal width	[0x24, 0x25]	HW[11:4] = 0x24 HW[3:0] = 0x25[7:4] HPAD[3:0] = 0x25[3:0] x 2
vertical height	[0x26, 0x27]	VH[11:4] = 0x26 VH[3:0] = 0x27[7:4] VPAD[3:0] = 0x27[3:0]

4.3 test pattern

For testing purposes, the OV2643 offers one type of test pattern, color bar.

figure 4-3 test pattern



color bar

table 4-3 test pattern selection control

function	register	description
color bar	0x43	Bit[7]: color bar enable 0: color bar OFF 1: color bar enable

4.4 AEC/AGC algorithms

4.4.1 overview

The Auto Exposure Control (AEC) and Auto Gain Control (AGC) allows the image sensor to adjust the image brightness to a desired range by setting the proper exposure time and gain applied to the image. Besides automatic control, exposure time and gain can be set manually from external control. The related registers are listed in **table 4-4**.

table 4-4 AEC/AGC control functions

function	register	description
AEC enable	0x13	Bit[1]: auto/manual exposure control select 0: manual 1: auto
AEC exposure time	{0x02, 0x03}	AEC[15:8] = 0x02[7:0] AEC[7:0] = 0x03[7:0]
AGC gain	0x01	AGC[7:0] = 0x01[7:0]
AGC enable	0x13	Bit[2]: auto/manual gain control select 0: manual 1: auto

4.4.2 average-based algorithm

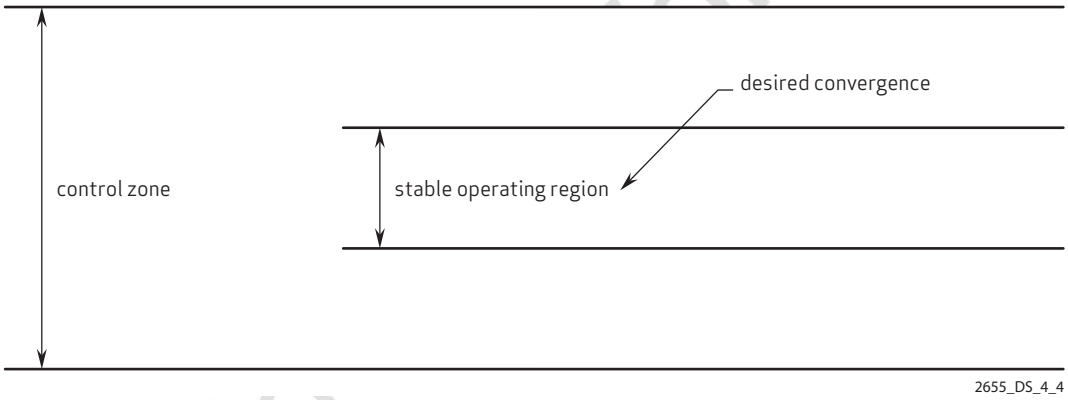
The average-based AEC controls image luminance using registers **WPT/HisH** (**0x18**) and **BPT/HisL** (**0x19**). In average-based mode, the value of register **WPT/HisH** (**0x18**) indicates the high threshold value and the value of register **0x19** (BPT/HisL) indicates the low threshold value. When the target image luminance average value **YAVG** (**0x1B**) is within the range specified by registers **WPT/HisH** (**0x18**) and **BPT/HisL** (**0x19**), the AEC maintains the image exposure (and gain). When register **YAVG** (**0x1B**) is greater than the value in register **WPT/HisH** (**0x18**), the AEC will decrease the image exposure and/or gain. When register **YAVG** (**0x1B**) is less than the value in register **BPT/HisL** (**0x19**), the AEC will increase the image exposure and/or gain. Accordingly, the value in register **WPT/HisH** (**0x18**) should be greater than the value in register **BPT/HisL** (**0x19**). The gap between the values of registers **WPT/HisH** (**0x18**) and **BPT/HisL** (**0x19**) controls the image stability.

The AEC function supports both normal and fast speed selections in order to bring the image exposure into the range set by the values in registers **WPT/HisH** (**0x18**) and **BPT/HisL** (**0x19**). AEC set to normal mode will allow for single-step increment or decrement in the image exposure to maintain the specified range. AEC set to fast mode will provide for an approximate ten-step increment or decrement in the image exposure to maintain the specified range. A value of "0" in register Auto_1[7] (**0x13**) will result in normal speed operation and a "1" will result in fast speed operation.

Register **VPT** (**0x1A**) controls the fast AEC range. If the target image **YAVG** (**0x1B**) is greater than **0x1A**[7:4] × 16, AEC will decrease by 2. If register **YAVG** (**0x1B**) is less than **0x1A**[3:0] × 16, AEC will increase by 2.

As shown in **figure 4-4**, the AEC/AGC convergence uses two regions, the inner stable operating region and the outer control zone.

figure 4-4 desired convergence



Control Zone Upper Limit: {**VPT**[7:4] (**0x1A**[7:4]), 4'b0000}

Control Zone Lower Limit: {**VPT**[3:0] (**0x1A**[3:0]), 4'b0000}

Stable Operating Region Upper Limit: WPT[7:0] (**0x18**)

Stable Operating Region Lower Limit: BPT[7:0] (**0x19**)

table 4-5 AEC control functions

function	register	description
WPT/HisH	0x18	luminance signal high range for AEC/AGC operation AEC/AGC value decreases in auto mode when average luminance histogram is greater than WPT/HisH[7:0].
BPT/HisL	0x19	luminance signal low range for AEC/AGC operation AEC/AGC value increases in auto mode when average luminance histogram is less than BPT/HisL[7:0].
VPT	0x1A	fast mode large step range thresholds - effective only in AEC/AGC fast mode Bit[7:4]: high threshold Bit[3:0]: low threshold AEC/AGC may change in larger steps when luminance average is greater than {VPT[7:6], 4'b0000} or less than {VPT[3:0],4'b0000}
YAVG	0x1B	luminance average - this register will auto update. Average luminance is calculated from the B/Gb/Gr/R channel average as follows: B/Gb/Gr/R channel average = (BAVG[7:0] + GbAVG[7:0] + GrAVG[7:0] + RAVG[7:0]) x 0.25
fast AEC enable	0x13	Bit[7]: AEC speed select 0: average-based AEC/AGC 1: histogram-based AEC/AGC

For the average-based AEC/AGC algorithm, the measured window is horizontally and vertically adjustable and divided by sixteen (4x4) zones (see **figure 4-5**). Each zone (or block) is 1/16th of the image and has a 2-bit weight in calculating the average luminance (YAVG). The final YAVG is the weighted average of the sixteen zones. The 2-bit weight could be n/4 where n is 0, 1, 2 or 4. For more details on adjusting horizontal and vertical windows and weight for each window, refer to **section 4.4.2.1,** average luminance (YAVG).

4.4.2.1 average luminance (YAVG)

Auto exposure time calculation is based on a frame brightness average value. By properly setting HS, VS, HW, and VH as shown in **figure 4-5**, a 4x4 grid window is defined. The value is the weighted average of the 16 sections. **table 4-6** lists the corresponding registers.

figure 4-5 average-based window definition

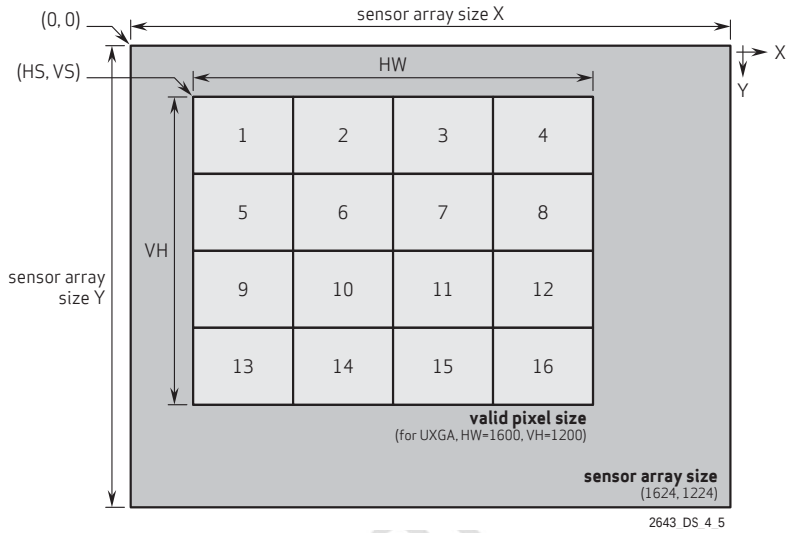


table 4-6 average-based algorithm functions

function	register	description
horizontal starting pixel (HS)	{0x20, 0x21}	HS[11:8] = 0x20[3:0] HS[7:0] = 0x21[7:0]
vertical starting pixel (VS)	{0x22, 0x23}	VS[11:8] = 0x22[3:0] VS[7:0] = 0x23[7:0]
section width (HW)	{0x24, 0x25}	HW[11:8] = 0x24[3:0] HW[7:0] = 0x25[7:0]
section height (VH)	{0x26, 0x27}	VH[11:8] = 0x26[3:0] VH[7:0] = 0x27[7:0]
section weighting	0x9B~0x9E	section 1 weight = 0x9B[7:6] section 2 weight = 0x9B[5:4] section 3 weight = 0x9B[3:2] section 4 weight = 0x9B[1:0] section 5 weight = 0x9C[7:6] section 6 weight = 0x9C[5:4] section 7 weight = 0x9C[3:2] section 8 weight = 0x9C[1:0] section 9 weight = 0x9D[7:6] section 10 weight = 0x9D[5:4] section 11 weight = 0x9D[3:2] section 12 weight = 0x9D[1:0] section 13 weight = 0x9E[7:6] section 14 weight = 0x9E[5:4] section 15 weight = 0x9E[3:2] section 16 weight = 0x9E[1:0]

4.5 AEC/AGC steps

The AEC and AGC work together to obtain adequate exposure/gain based on the current environmental illumination. In order to achieve the best SNR, extending the exposure time is always preferred to raising the analog gain when the current illumination is going brighter. Vice versa, under bright conditions, the action to decrease the gain is always taken prior to shorten the exposure time.

4.5.1 auto exposure control (AEC)

The function of the AEC is to calculate integration time of the next frame and send the information to the timing control block. Based on the statistics of previous frames, the AEC is able to determine whether the integration time should increase, decrease, fast increase, fast decrease, or remain the same.

In extremely bright situations, the LAEC activates, allowing integration time to be less than one row period. In extremely dark situations, the VAEC activates, allowing integration time to be larger than one frame period.

To avoid image flickering under a periodic light source, the integration time step can be adjusted as an integer multiple of the period of the light source. This new AEC step system is called banding, suggesting that the steps are not continuous but fall in some bands.

4.5.1.1 LAEC

If the integration time is only one row but the image is too bright, AEC will enter LAEC mode. Within LAEC, the integration time can be further decreased to the minimal of 1/16 row or so. LAEC ON/OFF can be set in 0x13[3].

4.5.1.2 banding mode ON with AEC

In Banding ON mode, AEC step, which is also called 'band', increments by an integer multiple of the period of light intensity. This design is to reject image flickering when light source is not steady but periodical.

For a given operating frequency, band step can be expressed in terms of row timing.

Band Step = 'period of light intensity' x 'frame rate' x 'rows per frame'.

The band steps can be set in registers 0x1E~0x1F.

When auto-banding is ON, if the next integration time is less than the minimal band step, banding will automatically turn OFF. It will turn ON again until the next integration time becomes larger than minimal band. If auto-banding is disabled, the minimal integration time is one minimal band. Auto-banding can be set in 0x13[4].

4.5.1.3 banding mode OFF with AEC

When Banding is OFF, integration time increases/decreases by 1/16 of the previous step in slow mode or becomes twice/half of the previous step in fast mode.

4.5.1.4 VAEC

In extremely dark situations, the integration time needs to be longer than one frame.

The OV2643 supports long integration time such as 2 frames, 3 frames, 4 frames, 5 frames, 6 frames, 7 frames, and 8 frames. This is achieved by slowing down original frame rate and waiting for exposure. VAEC ceiling can be set in 0x14[2:0]. VAEC can be disabled by setting 0x14[3] to 0.

4.5.2 auto gain control (AGC)

Unlike prolonging integration time, increasing gain will amplify both signal and noise or between two gaps of banding exposure time. Thus, AGC usually starts after AEC is full. However, in cases where adjacent AEC step changes are too large (>1/16), AGC steps should be inserted in between; otherwise, the integration time will keep switching between two adjacent steps and the image flickers.

4.5.2.1 integration time between 1~16 rows

When integration time is less than 16 rows, the changes between adjacent AEC steps are larger than 1/16, which could make the image oscillate between two AEC levels. Thus, some AGC steps are added in between. For example, from AEC = 2 row to AEC = 3 rows, there are 7 more AGC steps (1+ x/16, x=1~7) inserted, which ensures every step change is less than 1/16.

4.5.2.2 gain insertion between AEC banding steps

In Banding ON mode, the minimal integration time change is the period of light intensity (10ms for 50Hz, 16.67ms for 60Hz). For the first 16 band steps, since the change between adjacent step is larger than 1/16, AGC steps are inserted to ensure image stability.

4.5.2.3 gain insertion between VAEC steps

Between VAEC steps (e.g., integration time = 1 frame and 2 frames), AGC steps are inserted to ensure no adjacent step change is larger than 1/16 (6.25%).

4.5.2.4 when AEC reaches maximum

When AEC reaches its maximum while the image is still too dark, AGC starts to increase until new frame average falls into the no-adjust region or AGC reaches its maximum. The AGC maximum can be set in 0x15[2:0].

table 4-7 histogram-based AEC/AGC reference area option (sheet 1 of 2)

function	register	description
LAEC ON/OFF	0x13	Bit[3]: LAEC ON/OFF select 0: OFF 1: ON
banding ON/OFF	0x13	Bit[5]: banding ON/OFF select 0: OFF 1: ON
VAEC ON/OFF	0x14	Bit[3]: VAEC ON/OFF select 0: OFF 1: ON
auto banding	0x13	Bit[4]: auto banding ON/OFF select 0: OFF 1: ON

table 4-7 histogram-based AEC/AGC reference area option (sheet 2 of 2)

function	register	description
max integration time	0x14	Bit[2:0]: VAEC ceiling 000: 1 frame 001: 2 frames 010: 3 frames 011: 4 frames 100: 5 frames 101: 6 frames 110: 7 frames 111: 8 frames
max_band	0x1D	Bit[5:0]: max banding in terms of row exposure
banding step	{0x1E, 0x1F}	BDST[9:8] = 0x1E[1:0] BDST[7:0] = 0x1F[7:0]

4.6 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines. These lines are used to provide the data for black level calibration.

Black level adjustments can be made with registers 0x2F through 0x36.

table 4-8 BLC control functions

function	register	description
target	0x36	Bit[7:0]: target black level value that is used in the algorithm
	0x35	Bit[7:0]: set to same value as 0x36[7:0]
MBLC	0x2F	Bit[0]: When set, triggers BLC manually for 1 frame
BLCX2	0x2F	Bit[7]: when set, BLC will be triggered when the gain is changing (high gain)

4.7 digital gain

After black level subtraction, multiplication may apply to all pixel values based on an optional digital gain. By default, the sensor will use analog gain up to its maximum before applying digital gain to the pixels.

5 image sensor processor digital functions

5.1 ISP_TOP

The ISP_TOP includes all module enable signals, buffer power down and cen control, top level control signals as well as ISP modules that require control bytes (DPC, UV_AVG, and pre-ISP).

- DPC: Defective Pixel Canceling is used to detect and remove white and black defect pixels.
- UV_AVG: The U and V average module is used to smooth chrominance to let color image looks better around edge. It has two options to do: average with five consecutive U or V and get median value from five consecutive U or V.
- pre-ISP: This module is used to latch data, crop window, append dummy lines and create pixel order signal for ISP data path. It can also generate some test patterns for debug, such as color bar, color or black square block and random image.

table 5-1 ISP_TOP-related registers (sheet 1 of 2)

address	default value	R/W	function
0x40	0xFB	RW	ISP Control (bypass ISP and enable pins in RAW path) Bit[7]: ISP enable Bit[6]: RAW gamma enable Bit[5]: AWB statistic enable Bit[4]: AWB gain enable Bit[3]: LENC enable Bit[2]: LCD adjustment enable Bit[1]: Black pixel canceling enable Bit[0]: White pixel canceling enable
0x41	0x17	RW	ISP Control (enable pins in YUV path) Bit[7:6]: Reserved Bit[5]: UV_AVG select 0: 5 point median filter 1: 5 point average filter Bit[4]: LENC gain adjust enable Bit[3]: SDE enable Bit[2]: UV_AVG enable Bit[1]: CMX enable Bit[0]: CIP enable
0x42	0x00	RW	ISP Control (0: disable; 1: enable) Bit[7:3]: Reserved Bit[2]: Read-only latch select for indirect read 0: vsync_rise 1: AWB_done Bit[1]: Average option for AEC 0: (5R + 9G + 2B) / 16 1: (R + G + B) / 3 Bit[0]: Reserved

table 5-1 ISP_TOP-related registers (sheet 2 of 2)

address	default value	R/W	function
0x43	0x00	RW	Pre_ISP Control Bit[7]: ISP test enable Bit[6]: ISP test Rolling horizontal bar enable Bit[5]: ISP test Transparent mode (test image + real image) Bit[4]: ISP test ISP input data low bits = 0 Bit[3:2]: Color bar style 00: Normal color bar 01: Vertical changed color bar 10: Horizontal changed color bar 11: Vertical changed color bar mode 2 Bit[1:0]: ISP test Select different test patterns 00: Color bar 01: Random data 10: Squares 11: Black image
0x44	0x10	RW	Pre_ISP Control Bit[7:6]: Reserved Bit[5]: ISP test Square select 0: Color square 1: BW square Bit[4]: ISP test Random image reset enable (every frame is same) Bit[3:0]: ISP test Random image seed
0x46	0x04	RW	Bit[7:0]: BLC target manual value
0x47	0x3F	RW	Bit[7]: bias_man_en Bit[6]: Reserved Bit[5]: LENC_bias_plus Bit[4]: LENC_bias_on Bit[3]: GMA_bias_plus Bit[2]: GMA_bias_on Bit[1]: LCD_bias_plus Bit[0]: LCD_bias_on

5.2 lens correction (LENC)

The main purpose of the Lens Correction (LENC) function is to compensate for lens imperfection. According to the radius of each pixel to the lens center, the module calculates a gain for the pixel, correcting each pixel with its gain calculated to compensate for the light distribution due to lens curvature.

table 5-2 LENC-related registers (sheet 1 of 2)

address	default value	R/W	function
0x3E	0x04	RW	LENCX Bit[7:0]: Offset between sensor output image left most pixel and pixel array left most position
0x3F	0x02	RW	LENCY Bit[7:0]: Offset between sensor output image upper most pixel and pixel array upper most position
0x4C	0x03	RW	R Center X High Bits Bit[7:3]: Reserved Bit[3:0]: R_X0[10:8]
0x4D	0x30	RW	R Center X Low Bits Bit[7:0]: R_X0[7:0]
0x4E	0x02	RW	R Center Y High Bits Bit[7:3]: Reserved Bit[3:0]: R_Y0[10:8]
0x4F	0x5C	RW	R Center Y Low Bits Bit[7:0]: R_Y0[7:0]
0x50	0x00	RW	Bit[7]: Reserved Bit[6:0]: R_A1[6:0]
0x51	0x00	RW	Bit[7:0]: R_B1
0x52	0xFF	RW	Bit[7:4]: R_B2[3:0] Bit[3:0]: R_A2[3:0]
0x53	0x03	RW	G Center X High Bits Bit[7:3]: Reserved Bit[3:0]: G_X0[10:8]
0x54	0x30	RW	G Center X Low Bits Bit[7:0]: G_X0[7:0]
0x55	0x02	RW	G Center Y High Bits Bit[7:3]: Reserved Bit[3:0]: G_Y0[10:8]
0x56	0x5C	RW	G Center Y Low Bits Bit[7:0]: G_Y0[7:0]

table 5-2 LENC-related registers (sheet 2 of 2)

address	default value	R/W	function
0x57	0x00	RW	Bit[7]: Reserved Bit[6:0]: G_A1[6:0]
0x58	0x00	RW	Bit[7:0]: G_B1
0x59	0xFF	RW	Bit[7:4]: G_B2[3:0] Bit[3:0]: G_A2[3:0]
0x5A	0x03	RW	B Center X High Bits Bit[7:3]: Reserved Bit[3:0]: B_X0[10:8]
0x5B	0x30	RW	B Center X Low Bits Bit[7:0]: B_X0[7:0]
0x5C	0x02	RW	B Center Y High Bits Bit[7:3]: Reserved Bit[3:0]: B_Y0[10:8]
0x5D	0x5C	RW	B Center Y Low Bits Bit[7:0]: B_Y0[7:0]
0x5E	0x00	RW	Bit[7]: Reserved Bit[6:0]: B_A1[6:0]
0x5F	0x00	RW	Bit[7:0]: B_B1
0x60	0xFF	RW	Bit[7:4]: B_B2[3:0] Bit[3:0]: B_A2[3:0]
0x61	0x0C	RW	Bit[7:5]: Reserved Bit[4:0]: Gain high threshold
0x62	0x06	RW	Bit[7]: Gain coefficient manual mode enable Bit[6:5]: Reserved Bit[4:0]: Gain low threshold
0x63	0x80	RW	Bit[7:0]: Coefficient threshold
0x64	0x80	RW	Bit[7:0]: Coefficient manual value

5.3 gamma

Gamma converts the pixel values according to the Gamma curve to compensate the sensor output under different light strengths. The non-linear gamma curve is approximately constructed with different linear functions.

table 5-3 gamma registers

address	default value	R/W	function	
0x65	0x05	RW	Bit[7:0]	YST1
0x66	0x0C	RW	Bit[7:0]	YST2
0x67	0x1C	RW	Bit[7:0]	YST3
0x68	0x2A	RW	Bit[7:0]	YST4
0x69	0x29	RW	Bit[7:0]	YST5
0x6A	0x45	RW	Bit[7:0]	YST6
0x6B	0x52	RW	Bit[7:0]	YST7
0x6C	0x5D	RW	Bit[7:0]	YST8
0x6D	0x68	RW	Bit[7:0]	YST9
0x6E	0x7F	RW	Bit[7:0]	YST10
0x6F	0x91	RW	Bit[7:0]	YST11
0x70	0xA5	RW	Bit[7:0]	YST12
0x71	0xC6	RW	Bit[7:0]	YST13
0x72	0xDE	RW	Bit[7:0]	YST14
0x73	0xEF	RW	Bit[7:0]	YST15
0x74	0x16	RW	Bit[7:0]	YSLP (when sub register **0xB5**[2] = 0, this value is automatically calculated)

5.4 auto white balance (AWB)

The main purpose of the Auto White Balance (AWB) function is to automatically correct the white balance of the image. There are two main functions AWB: AWB_Stat and AWB_Gain.

- AWB_Stat is used to automatically generate digital gain for different light sources
- AWB_Gain is used to apply the AWB_Stat gain information on RAW data to remove unrealistic color

table 5-4 AWB-related registers (sheet 1 of 2)

address	default value	R/W	function
0x75	0x5C	RW	AWB Control 1 Bit[7:6]: STEP_FAST[1:0] (when sub register 0x77[7] = 1) Bit[5:4]: STEP_LOCAL[1:0] Bit[3]: G_EN Bit[2]: AWB_SIMPLE Bit[1:0]: Advanced AWB control
0x76	0x00	RW	AWB Control 2 Bit[7:4]: MAX_FAST_CNT[3:0] (when sub register 0x77[7] = 1) Bit[3:0]: MAX_LOCAL_CNT[3:0]
0x77	0x92	RW	AWB Control 3 Bit[7]: FAST_ENABLE Bit[6:4]: COUNT_LIMIT_CTRL[2:0] Bit[3:0]: STABLE_RANGE[3:0]
0x78	0x21	RW	AWB Control 4 Bit[7:6]: COUNT_AREA_SEL[1:0] Bit[5]: AWB_SIM_SEL 0: After AWB gain module 1: After gamma module Bit[4]: AWB_RBLUE Bit[3:0]: Advanced AWB control
0x79	0xE0	RW	AWB Control 5 Bit[7]: AWB_SIMF Only for simple AWB BIT[6]: AWB_BIAS_PLUS Bit[5]: AWB_BIAS_ON BIt[4]: AWB_BIAS_STAT Bit[3]: AWB_FREEZE Bit[4]: AWB_PRESET BIt[3:2]: AWB_WIN Select different cropping windows
0x7A	0x02	RW	Bit[7:0]: LOCAL_LIMIT
0x7B	0xFF	RW	Bit[7:0]: AWB_B_BLOCK
0x7C~0x88	–	RW	Advanced AWB Control Registers

table 5-4 AWB-related registers (sheet 2 of 2)

address	default value	R/W	function
0x89	0xF0	RW	Bit[7:0]: RED_LIMIT
0x8A	0xF0	RW	Bit[7:0]: GREEN_LIMIT
0x8B	0xF0	RW	Bit[7:0]: BLUE_LIMIT
0x8C	0x40	RW	Bit[7:0]: LCD_R_COEF
0x8D	0x40	RW	Bit[7:0]: LCD_G_COEF
0x8E	0x40	RW	Bit[7:0]: LCD_B_COEF

5.5 defect pixel canceling (DPC)

The main purpose of the Defect Pixel Canceling (DPC) function is to automatically remove the white and black defect pixels in the image. Connected pixels can also be removed if register bits 0x8F[4] and 0x8F[3] are enabled.

table 5-5 DPC-related registers

address	default value	R/W	function
0x40	2'b11	RW	Bit[1]: Black pixel canceling enable Bit[0]: White pixel canceling enable
0x8F	0x1C	RW	Bit[7:5]: Reserved Bit[4:0]: Debug control Changing these registers is not recommended

5.6 color interpolation (CIP), DNS and sharpen

The color interpolation (CIP) functions include de-noising of raw images, RAW to RGB interpolation, and edge enhancement. CIP functions work in both manual and auto modes.

figure 5-1 DNS_TH diagram

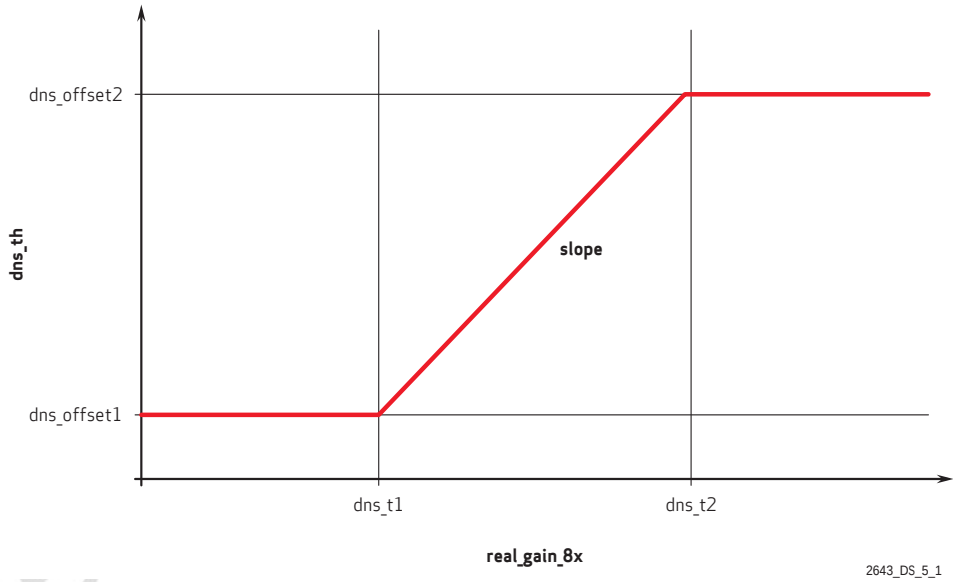


figure 5-2 sharpen_MT diagram

figure 5-3 sharpen_TH diagram

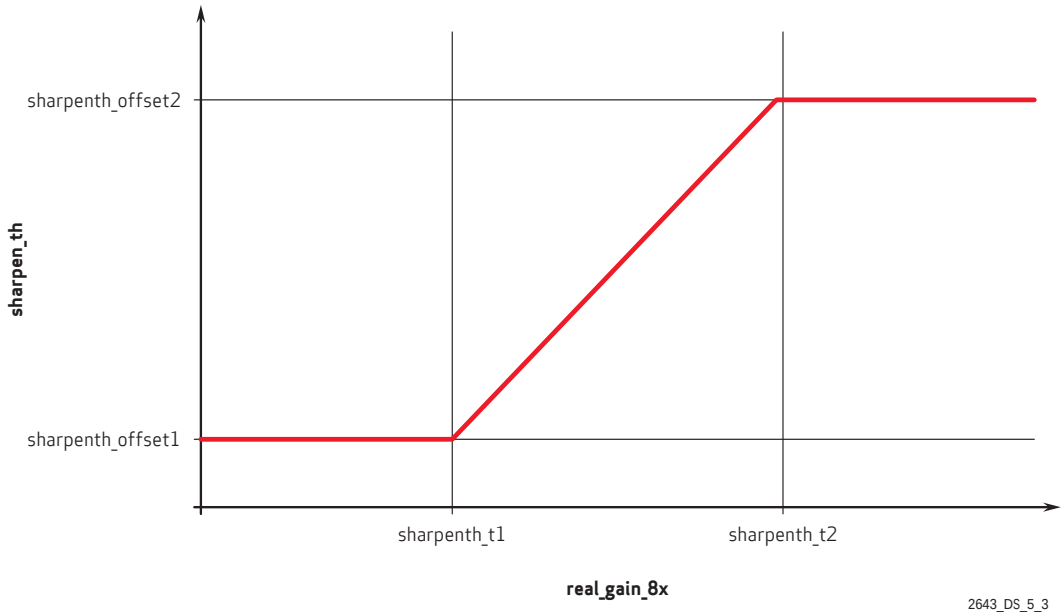


table 5-6 CIP, DNS, sharpen-related registers (sheet 1 of 2)

address	default value	R/W	function	
0x9F	0x08	RW	Bit[7:0]	SHARPENMT_T1 Low gain threshold for calculating sharpen strength automatically, T1<T2)
0xA0	0x48	RW	Bit[7:0]:	SHARPENMT_T2 High gain threshold for calculating sharpen strength automatically, T1<T2)
0xA1	0x18	RW	Bit[7]: Bit[6:0]:	Reserved SHARPENMT_OFFSET1[6:0] / MANUAL SHARPEN THRESHOLD Maximum sharpen strength in auto mode, shared with manual sharpen strength
0xA2	0x0E	RW	Bit[7] Bit[6:0]	Reserved SHARPENMT_OFFSET2[6:0] Minimum sharpen strength in auto mode, Offset1>Offset2
0xA3	0x08	RW	Bit[7:0]	DNS_T1 Low gain threshold for calculating denoise threshold automatically, T1<T2

table 5-6 CIP, DNS, sharpen-related registers (sheet 2 of 2)

address	default value	R/W	function
0xA4	0x48	RW	Bit[7:0]: DNS_T2 High gain threshold for calculating denoise threshold automatically, T1<T2
0xA5	0x09	RW	Bit[7]: Reserved Bit[6:0]: DNS_OFFSET1[6:0] / MANUAL DNS THRESHOLD Maximum denoise threshold in auto mode, shared with manual denoise threshold
0xA6	0x16	RW	Bit[7]: Reserved Bit[6:0]: DNS_OFFSET2[6:0] Minimum denoise threshold in auto mode, Offset1<Offset2
0xA7	0x08	RW	Bit[7:0] SHARPENTH_T1 Low gain threshold for calculating sharpen threshold automatically, T1<T2
0xA8	0x48	RW	Bit[7:0] SHARPENTH_T2 High gain threshold for calculating sharpen threshold automatically, T1<T2
0xA9	0x04	RW	Bit[7] SHARPEN_MAN_EN Bit[6] CIP_BOUNDARY_EN Bit[5] DNS_MAN_EN Bit[4:0] SHARPENTH_OFFSET1 / MANUAL SHARPENTH THRESHOLD Maximum sharpen threshold in auto mode, shared with manual sharpen threshold
0xAA	0xA6	RW	Bit[7:5] THRE_RB_SHARPEN Bit[4:0]: SHARPENTH_OFFSET2 Minimum sharpen threshold in auto mode, Offset1<Offset2

5.7 color matrix (CMX)

The main purpose of the Color Matrix (CMX) function is to convert images from the RGB domain to YUV domain.

table 5-7 CMX-related registers

address	default value	R/W	function
0xAB	0x33	RW	Bit[7:0] CMX1
0xAC	0x41	RW	Bit[7:0] CMX2
0xAD	0x0F	RW	Bit[7:0] CMX3
0xAE	0x0B	RW	Bit[7:0] CMX4
0xAF	0x44	RW	Bit[7:0] CMX5
0xB0	0x50	RW	Bit[7:0] CMX6
0xB1	0x55	RW	Bit[7:0] CMX7
0xB2	0x3A	RW	Bit[7:0] CMX8
0xB3	0x1C	RW	Bit[7:0] CMX9
0xB4	0x98	RW	Bit[7:0] CMX_sign[7:0] Sign bits for CMX1 to CMX8
0xB5	0x21	RW	Bit[7:6]: Reserved Bit[5]: UV_adjust_TH2[8] Bit[4]: ADJ_man_i Bit[3]: Y_avg_man Bit[2]: gamma_man Bit[1]: CMX_double Bit[0]: CMX_sign[8] Sign bit for CMX9

5.8 special digital effects (SDE) and UV adjust (UV_ADJ)

The Special Digital Effects (SDE) functions include hue/saturation control, brightness, contrast, etc. Use SDE_CTRL to add some special effects to the image. Calculate the new U and V from Hue Cos, Hue Sin, and parameter signs. Saturate U and V manually using the Sat_u and Sat_v registers. The UV adjust module is merged with the saturate UV function. Calculate Y using Y offset, Y gain, and Y bright or set the Y value. SDE supports negative, black/white, sepia, greenish, blueish, reddish and other image effects which combine the effects already listed.

UV adjust (UV_ADJ) is used to reduce chrominance values in low light conditions to improve image quality. The higher AGC gain is, the lower the chrominance values. UV_ADJ has an automatic and manual mode, where the latter is equal to the above manual UV saturation.

figure 5-4 UV adjust value diagram

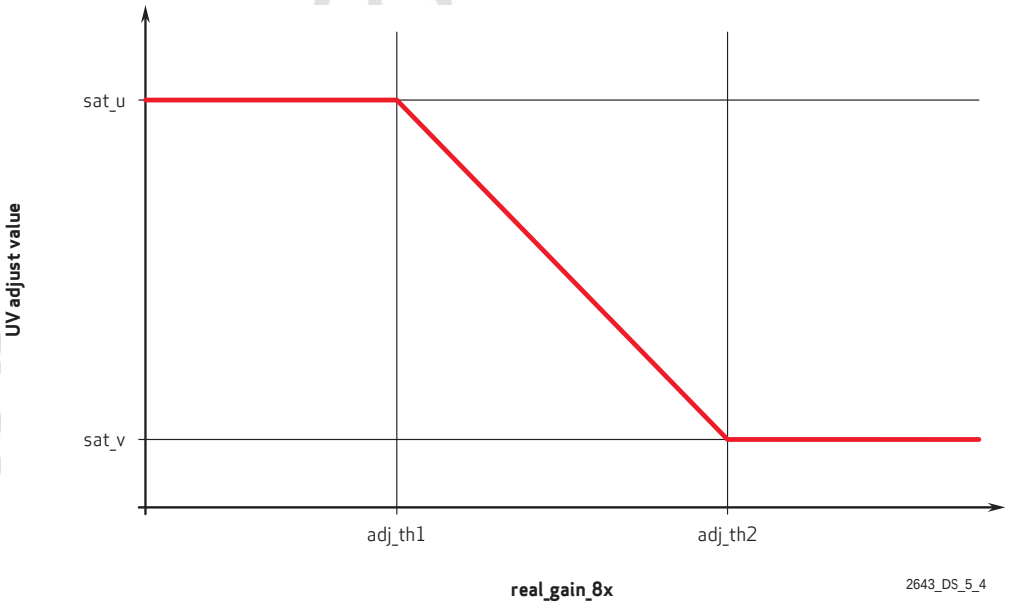


table 5-8 UV_ADJ-related registers (address base: 0x338B)

address	default value	R/W	function
0xB5	1'b1	RW	Bit[5]: UV adjust TH2[8] (UV_adjust_TH2[7:0] is at 0xC0[7:0])
0xB6	0x00	RW	SDE_Ctrl[7:0] Bit[7]: Fixed_Y_en Bit[6]: Negative_en Bit[5]: Gray_en Bit[4]: Fixed_U_en Bit[3]: Fixed_V_en Bit[2]: Y_contrast_en Bit[1]: Saturate_en Bit[0]: Hue_en
0xB7	0x80	RW	Bit[7:0] HUE_COS
0xB8	0x00	RW	Bit[7:0] HUE_SIN
0xB9	0x40	RW	Bit[7:0]: SAT_U / FIXED_U
0xBA	0x40	RW	Bit[7:0]: SAT_V / FIXED_V
0xBB	0x80	RW	Bit[7:0]: Manual Y offset
0xBC	0x80	RW	Bit[7:0]: Y contrast gain (20 = 1x)
0xBD	0x00	RW	Bit[7:0]: YBRIGHTNESS
0xBE	0x01	RW	Bit[7:6]: Reserved Bit[5:0]: SGNSET[5:0] Hue: SGN0=1, SGN1=0, SGN4=SGN5=0 => $0<\theta<\pi/2$ SGN0=0, SGN1=1, SGN4=SGN5=0 => $-\pi/2<\theta<0$ SGN0=1, SGN1=0, SGN4=SGN5=1 => $-\pi/2<\theta<\pi$ SGN0=0, SGN1=1, SGN4=SGN5=1 => $-\pi<\theta<-\pi/2$ Y_contrast: SGN2: YOFFSET SGN3: YBRIGHTNESS
0xBF	0x10	RW	Bit[7:0]: UV_adjust TH1
0xC0	0x00	RW	Bit[7:0]: UV_adjust TH2[7:0] (UV_adjust TH2[8] is at 0xB5[5])

5.9 format description

Format control converts internal data format into the desirable output format including YUV, RGB and raw.

table 5-9 format control register list

register address	register name	function
0x12	SYS	FMT_CTRL0 Bit[3:2]: Format selection 00: RAW 01: RGB 1x: YUV422
0x0D	DVP2	FMT_CTRL1 Bit[6:5]: YUV422 or GBR422 output sequence 00: YUYV.../GBGR... 01: YUVY.../BGRG... 10: YVYU.../GRGB... 11: VYUY.../RGBG... Bit[4]: RAW data selection 0: RAW data is from ISP 1: RAW data is from sensor Bit[3:2]: RGB data selection 00: RGB555, {1'b0, B[4:0], G[4:3]}, {G[2:0], R[4:0]} 01: RGB565, {B[4:0], G[5:3]}, {G[2:0], R[4:0]} 1x: GBR422, GB, GR.../BG, RG... (data order can be adjusted using 0x0D[6:5])
0x0C	DVP1	FMT_CTRL2 Bit[5]: CC656 0: Disable CC656 1: Enable CC656 Bit[3:2]: ISP RAW selection (when 0x0D[4] = 0) 00: RAW data after DPC 01: RAW data after LENC 10: RAW data after AWB 11: RAW data after gamma

6 image sensor output interface digital functions

6.1 digital video port (DVP)

6.1.1 overview

The Digital Video Port (DVP) provides 10-bit parallel data output in all formats supported, and extended features including test pattern output.

table 6-1 DVP-related registers

address	register name	function
0xC1	DVP_CTRL00	DVP Control 00 Bit[7:6]: Reserved for debug only Bit[5]: 10_3F0 0: No limit 1: Limit data between 0x10 and 0x3F0 in CC656 Bit[4]: 40_3C0 0: No limit 1: Limit data between 0x40 and 0x3C0 in C656 Bit[3]: DGB_OUT 0: Normal 1: Debug mode Bit[2]: BT_BIT8 0: Bit test pattern uses 10-bit data 1: Bit test pattern uses 8-bit data Bit[1]: BT_M1 0: Bit test pattern shifts one bit in every clock period 1: Bit test pattern shifts one bit in every two clock periods Bit[0]: BT_OUT 0: Output normal image 1: Output bit test pattern
0xC2	DVP_CTRL01	DVP Control 01 Bit[7:6]: DATA_ORDER 00: DVP output DVP_DATA[9:0] 01: DVP output DVP_DATA[0:9] 10: DVP output DVP_DATA{[2:9], [1:0]} 11: DVP output DVP_DATA{[7:0], [9:8]} Bit[5]: D_POL 0: Normal 1: Output bit is reversed Bit[4]: HREF_POL 0: Normal 1: HREF will be reversed Bit[3]: VSYNC_POL 0: Normal 1: VSYNC will be reversed Bit[2]: PCLK_POL 0: Normal 1: PCLK will be reversed Bit[1:0]: Reserved

6.1.2 DVP timing

note
Timing values shown in **table 6-2** may vary depending upon register settings.

figure 6-1 DVP timing diagram

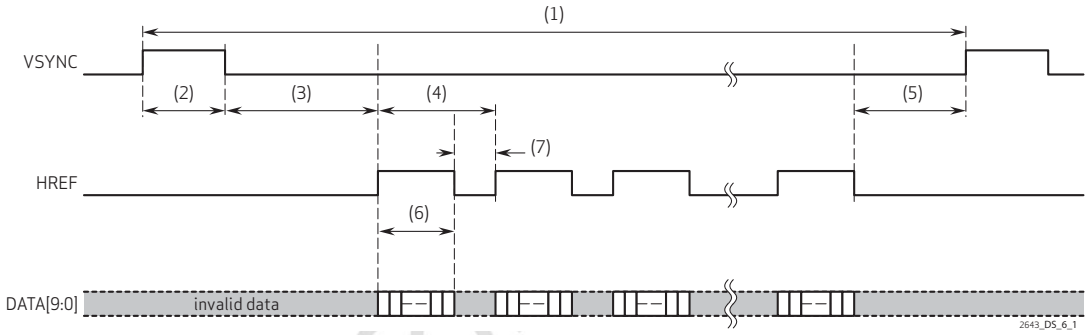


table 6-2 DVP timing specifications (sheet 1 of 2)

mode	max frame rate	format	timing
UXGA 1600 x 1200	15 fps	RAW	(1) 2398500 tp (2) 3900 tp (3) 23695 tp (4) 1950 tp (5) 30905 tp (6) 1600 tp (7) 350 tp
SVGA 800 x 600	30 fps	RAW	(1) 799500 tp (2) 2460 tp (3) 48110 tp (4) 1230 tp (5) 13090 tp (6) 800 tp (7) 430 tp
CIF 400 x 300	30 fps	RAW	(1) 600000 tp (2) 1500 tp (3) 366607 tp (4) 750 tp (5) 6893 tp (6) 400 tp (7) 350 tp
QCIF 200 x 150	30 fps	RAW	(1) 300000 tp (2) 750 tp (3) 183303 tp (4) 375 tp (5) 3447 tp (6) 200 tp (7) 175 tp

table 6-2 DVP timing specifications (sheet 2 of 2)

mode	max frame rate	format	timing
720p 1280 x 720	30 fps	RAW	(1) 1200000 tp (2) 3200 tp (3) 22697 tp (4) 1600 tp (5) 22424 tp (6) 1280 tp (7) 320 tp

6.1.3 DVP image formats

6.1.3.1 YUV422 format

Uncompressed YUV422 data is sent out through DATA[9:2] and the sequence can be YUYV, UYVY, YVYU, VYUY.

table 6-3 YUYV format

DATA[9:2]	first pixel	first pixel	second pixel	second pixel	third pixel	third pixel
even	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]
odd	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]

table 6-4 UYVY format

DATA[9:2]	first pixel	first pixel	second pixel	second pixel	third pixel	third pixel
even	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]
odd	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]

table 6-5 YVYU format

DATA[9:2]	first pixel	first pixel	second pixel	second pixel	third pixel	third pixel
even	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]
odd	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]

table 6-6 VYUY format

DATA[9:2]	first pixel	first pixel	second pixel	second pixel	third pixel	third pixel
even	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]
odd	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]

6.1.3.2 RGB565 format

Uncompressed RGB565 data is sent out through DATA[9:2].

table 6-7 RGB565 format

bytes	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2
even	R7	R6	R5	R4	R3	G7	G6	G5
odd	G4	G3	G2	B7	B6	B5	B4	B3

6.1.3.3 RGB555 format

table 6-8 RGB555 format

bytes	DATA9	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2
even	0	R7	R6	R5	R4	R3	G7	G6
odd	G5	G4	G3	B7	B6	B5	B4	B3

7 register tables

The following tables provide descriptions of the device control registers contained in the OV2643. For all register enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x60 for write and 0x61 for read.

table 7-1 system control registers (sheet 1 of 21)

address	register name	default value	RW	description
0x00	RSVD	–	–	Reserved
0x01	AGC	0x00	RW	Bit[7:0]: Gain value Maximum gain = 16x
0x02	AEC	0x00	RW	Bit[7:0]: Exposure value[15:8]
0x03	AEC	0x80	RW	Bit[7:0]: Exposure value[7:0]
0x04	LAEC	0x00	RW	Bit[7:0]: Less than one line exposure Exposure time = (HTS[15:0] - LAEC[7:0] x 8) T_{sysclk} where HTS is horizontal total timing length, defined in register {0x29, 0x2A} Limitation: Full Size: 52 ≤ LAEC[7:0] ≤ HTS[15:0] - 28 Down sample: 68 ≤ LAEC[7:0] ≤ HTS[15:0] - 40
0x05	RED	0x40	RW	Bit[7:0]: AWB gain red[11:4]
0x06	GREEN	0x40	RW	Bit[7:0]: AWB gain green[11:4]
0x07	BLUE	0x40	RW	Bit[7:0]: AWB gain blue[11:4]
0x08	RG	0x00	RW	Bit[7:4]: AWB gain red[3:0] Bit[3:0]: AWB gain green[3:0]
0x09	BLUE	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: AWB gain blue[3:0]
0x0A	PIDH	0x26	R	Bit[7:0]: Product ID MSB
0x0B	PIDL	0x43	R	Bit[7:0]: Product ID LSB

table 7-1 system control registers (sheet 2 of 21)

address	register name	default value	RW	description
0x0C	DVP1	0x00	RW	Bit[7]: 900p 0: Select image size 1280x720, valid only in crop mode (when register 0x12[6] = 1) 1: Select image size 1600x900, valid only in crop mode (when register 0x12[6] = 1) Bit[6]: sub_opt Bit[5]: cc656_en 0: CC656 disabled 1: CC656 enabled Bit[4]: gdvpck 0: DVP clock is free running 1: DVP clock is gated during blanking output Bit[3:2]: dsp_raw_sel 00: Select raw data after DPC 01: Select raw data after LENC 10: Select raw data after AWB 11: Select raw data after gamma Bit[1:0]: yavg_sel 00: Select frame average of sensor raw data 01: Select frame average of LENC output 10: Select frame average of AWB output 11: Select frame average of gamma output
0x0D	DVP2	0x14	RW	Bit[7]: Reserved Bit[6:5]: YUV/RGB output sequence select 00: YUYV/GBGR 01: UYVY/BGRG 10: YVYU/GRGB 11: VYUY/RGBG Bit[4]: sensor_raw 0: Select ISP raw data when output is raw 1: Select sensor raw data when output is raw Bit[3:2]: RGB_sel 00: RGB555 01: RGB565 1x: GBR422 Bit[1:0]: REG2D 2-bit register, can be output through GPIO[1:0] for special purposes
0x0E	PLL1	0x9C	RW	Bit[7:6]: bitdiv 00: bit8div = 1 01: bit8div = 1 10: bit8div = 4 11: bit8div = 5 Bit[5:0]: plldiv

table 7-1 system control registers (sheet 3 of 21)

address	register name	default value	RW	description
0x0F	PLL2	0x28	RW	Bit[7:4]: scalediv 0000: 1 others: scalediv[3:0] x 2 Bit[3:2]: sysdiv 00: sysdiv = 1 01: sysdiv = 2 10: sysdiv = 8 11: sysdiv = 16 Bit[1:0]: freqdiv 00: freqdiv = 1 01: freqdiv = 1.5 10: freqdiv = 2 11: freqdiv = 3
0x10	PLL3	0x0B	RW	Bit[7]: PLL power down Bit[6]: PLL bypass 0: Select PLL output clock 1: Bypass PLL Bit[5:3]: PLL charge pump control Bit[2:0]: indiv 000: indiv = 1 001: indiv = 1.5 010: indiv = 2 011: indiv = 3 100: indiv = 2 101: indiv = 3 110: indiv = 4 111: indiv = 6
0x11	CLK	0x40	RW	Bit[7]: dpllen 0: Input = PLL clock 1 Input = PLL clock x 2 Bit[6]: slvpck 0: DVP clock is generated by internal divider 1: DVP clock is from PLL clock Bit[5:0]: div DVP clock = input / (2 x div + 1)

table 7-1 system control registers (sheet 4 of 21)

address	register name	default value	RW	description
0x12	SYS	0x00	RW	Bit[7]: Soft reset 0: Normal 1: Soft reset Bit[6]: Crop 0: Normal 1: Crop mode, can output image at size 1600x900 or 1280x720 Bit[5]: Mirror Bit[4]: Flip Bit[3:2]: format_sel 00: Raw data 01: RGB 1x: YUV Bit[1:0]: size_sel 00: Full (1600x1200) 01: 1:2 subsample (800x600) 10: 1:4 subsample (400x300) 11: 1:8 subsample (200x150)
0x13	AUTO1	0xFF	RW	Bit[7]: fast_en 0: Slow AEC/AGC 1: Fast AEC/AGC Bit[6]: bstp 0: Limit AEC max step to blanking line number 1: AEC step no limit Bit[5]: bandf_en 0: Disable banding filter 1: Enable banding filter Bit[4]: autobd 0: AEC always use banding step 1: Banding ON/OFF auto detect Bit[3]: L1AEC 0: Disable less than one line exposure 1: Enable less than one line exposure Bit[2]: AWB_gain 0: Use manual AWB gain from registers 0x05~0x09 1 AWB gain auto calculated Bit[1]: AEC_en 0: Disable auto exposure control 1: Enable auto exposure control Bit[0]: AGC_en 0 Disable auto gain control 1 Enable auto gain control

table 7-1 system control registers (sheet 5 of 21)

address	register name	default value	RW	description
0x14	AUTO2	0xA7	RW	Bit[7]: Band50 0: 60Hz banding 1: 50Hz banding Bit[6]: Reserved Bit[5]: bdsw_rst 0: Do not reset AEC/AGC when switching between 50Hz and 60Hz 1: Reset AEC/AGC when switching between 50Hz and 60Hz Bit[4]: add_lt_1f 0: Step of adding dummy frame is one frame length 1: Step of adding dummy frame is current banding value Bit[3]: addfm_en 0: Add dummy frame is disabled 1: Add dummy frame is enabled Bit[2:0]: af Maximum number of dummy frame can be inserted
0x15	AUTO3	0x42	RW	Bit[7:4]: stb_off AEC/AGC stable zone = (WPT + BPT)/2 ± stb_off Bit[3]: fzex 0: AEC/AGC can be auto updated in auto mode 1: Freeze exposure and gain value in auto mode Bit[2:0]: gain_ceiling Gain limitation max gain = $2^{(gain\_ceiling + 1)}$
0x16	AUTO4	0xA1	RW	Bit[7]: lg_opt Bit[6]: Reserved Bit[5:4]: hlg_opt Gain option when add dummy frame is enabled. Dummy frame can only be inserted after gain ≥ $2^{(hlg\_opt + 1)}$ Bit[3:2]: Reserved Bit[1:0]: sub_exp Option to set maximum exposure value of one frame

table 7-1 system control registers (sheet 6 of 21)

address	register name	default value	RW	description
0x17	AUTO5	0x40	RW	Bit[7:0]: MLAEC 0: Disable manual less than one line exposure 1: Enable manual less than one line exposure Bit[7:0]: AD128 0: ADC no 128 offset 1: ADC add 128 offset Bit[7:0]: AECG Exposure value in banding format Exposure = (AECG + 1) × banding step
0x18	WPT	0x78	RW	Bit[7:0]: AEC stable range high limit
0x19	BPT	0x68	RW	Bit[7:0]: AEC stable range low limit
0x1A	VPT	0xD4	RW	Bit[7:4]: AEC 2x high limit Exposure or gain will decrease by 2x step if frame average is larger than VPT[7:4] × 16 Bit[3:0]: AEC 2x low limit Exposure or gain will increase by 2x step if frame average is less than VPT[3:0] × 16
0x1B	YAVG	0x00	RW	Bit[7:0]: Frame average value
0x1C	VSOPT	0x22	RW	Bit[7]: Reserved Bit[6:4]: Adjust VSYNC start point Bit[3]: Reserved Bit[2:0]: Number of rows for VSYNC high pulse width
0x1D	AECGM	0x05	RW	Bit[7:6]: Reserved Bit[5:0]: Limitation of maximum banding exposure value (0x17[5:0])
0x1E	BDST	0x00	RW	Bit[7:0]: Banding step MSB
0x1F	BDST	0xB8	RW	Bit[7:0]: Banding step LSB
0x20	HS	0x01	RW	Bit[7:0]: Horizontal window start MSB
0x21	HS	0x24	RW	Bit[7:0]: Horizontal window start LSB
0x22	VS	0x00	RW	Bit[7:0]: Vertical window start MSB
0x23	VS	0x0A	RW	Bit[7:0]: Vertical window start LSB
0x24	HW	0x64	RW	Bit[7:0]: Horizontal window width bit[11:4]
0x25	HW	0x08	RW	Bit[7:4]: Horizontal window width bit[3:0] Bit[3:0]: Number of boundary pixels in horizontal window for DSP, each LSB represents two pixels
0x26	VH	0x4B	RW	Bit[7:0]: Vertical window height[11:4]

table 7-1 system control registers (sheet 7 of 21)

address	register name	default value	RW	description
0x27	VH	0x06	RW	Bit[7:4]: Vertical window height[3:0] Bit[3:0]: Number of boundary lines in vertical window for DSP, each LSB represents one line
0x28	HVOFF	0x42	RW	Bit[7:4]: Hoffset DSP output image horizontal start point: 2 x Hoffset Bit[3:0]: Voffset DSP output image vertical start point: Voffset
0x29	HTS	0x07	RW	Bit[7:0]: Number of clock periods for horizontal total timing length MSBs
0x2A	HTS	0x9E	RW	Bit[7:0]: Number of clock periods for horizontal total timing length LSBs
0x2B	VTS	0x04	RW	Bit[7:0]: Number of rows for vertical total timing MSBs
0x2C	VTS	0xCE	RW	Bit[7:0]: Number of rows for vertical total timing LSBs
0x2D	EXVTS	0x00	RW	Bit[7:0]: Dummy frame added MSBs Expressed in row number
0x2E	EXVTS	0x00	RW	Bit[7:0]: Dummy frame added LSBs Expressed in row number Dummy frame = EXVTS[15:0] / VTS[15:0]
0x2F	BLC	0xAC	RW	Bit[7]: blc_en 0: BLC is disabled 1: BLC is enabled Bit[6]: blc_always 0: Do BLC at gain change 1: Do BLC at every frame Bit[5:4]: Minimum gain change value to trigger BLC 00: 2x 01: Not allowed 10: 1.5x 11: 1.25x Bit[3]: blc_r 0: Black line do not include red line 1: Black line include red lines Bit[2]: blc_b 0: Black line do not include blue line 1: Black line include blue lines Bit[1]: latck_rev 0: Normal 1: Reverse clock edge to latch data from ADC Bit[0]: BLC_init 0: Normal 1: Trigger BLC for one frame, this bit will be reset to 0 after BLC finished

table 7-1 system control registers (sheet 8 of 21)

address	register name	default value	RW	description
0x30	BLC	0x00	RW	Bit[7:0]: BLC offset of B[7:0]
0x31	BLC	0x00	RW	Bit[7:0]: BLC offset of R[7:0]
0x32	BLC	0x00	RW	Bit[7:0]: BLC offset of Gb[7:0]
0x33	BLC	0x00	RW	Bit[7:0]: BLC offset of Gr[7:0]
0x34	BLC	0x00	RW	Bit[7:6]: BLC offset of B[9:8] Bit[5:4]: BLC offset of R[9:8] Bit[3:2]: BLC offset of Gb[9:8] Bit[1:0]: BLC offset of Gr[9:8]
0x35	OFFS	0x04	RW	Bit[7:0]: Offset Usually same as BLC target (register 0x36[7:0])
0x36	TARGET	0x04	RW	Bit[7:0]: BLC target
0x37	TMC0	0xE0	RW	Bit[7:5]: Reserved Bit[4]: fx 0: Normal 1: Drop VSYNC when drop frame is enabled Bit[3:2]: gplat_opt 00: SCCB group write before VSYNC 01: SCCB group write inside VSYNC 1x: SCCB group write after VSYNC Bit[1]: grpopt 0: No internal latch 1: Internal latch HTS, VTS Bit[0]: modchg 0: Do not reset system when changing format 1: reset system when changing format
0x38	TMC1	0x33	RW	Bit[7:5]: Reserved Bit[4]: blc_512 0: Black line max value no limit 1: Limit black line max value to 511 Bit[3]: rstyz_fixed 0: Data shift start point can be adjusted by register 0xC5 1: Data shift start point is fixed Bit[2:0]: cgain Gain compensation at less than one line exposure

table 7-1 system control registers (sheet 9 of 21)

address	register name	default value	RW	description
0x39	TMC2	0xD0	RW	Bit[7]: Hbin 0: Horizontal skip 1: Horizontal binning Bit[6]: Vbin 0: Vertical skip 1: Vertical binning Bit[5]: allhref 0: Normal 1: Delay VSYNC by 3ns Bit[4]: expng 0: AEC step no larger than blanking time 1: AEC step no limit Bit[3]: dropf_en 0: Disable drop frame function 1: Enable drop frame function Bit[2]: vslat_opt Adjust internal latch pulse start point Bit[1]: drop_vs 0: Disable drop VSYNC 1: Enable drop VSYNC Bit[0]: addvs_opt 0: Add dummy frame inside VSYNC 1: Add dummy frame before VSYNC
0x3A~ 0x3C	RSVD	–	–	Reserved
0x3D	TMC6	0x08	RW	Bit[7]: Reserved Bit[6]: Sleep 0: Normal 1: System enter sleep state (in this state, SCCB is still accessible) Bit[5]: hsynco 0: HREF is valid only during active pixel output 1: HREF is valid during frame blanking Bit[4]: Reserved Bit[3]: hvref_asft 0: HREF and VREF manually adjusted 1: HREF and VREF automatically shift by one pixel and one line, respectively at mirror and flip Bit[2:0]: Reserved
0x3E	LENCX	0x04	RW	Bit[7:0]: Offset between sensor output image left most pixel and pixel array left most position
0x3F	LENCY	0x02	RW	Bit[7:0]: Offset between sensor output image upper most line and pixel array upper most position

table 7-1 system control registers (sheet 10 of 21)

address	register name	default value	RW	description
0x40	REG40	0xFB	RW	Bit[7]: ISP enable Bit[6]: RAW gamma enable Bit[5]: AWB statistic enable Bit[4]: AWB_gain enable Bit[3]: LENC enable Bit[2]: LCD adjustment enable Bit[1]: Black pixel canceling enable Bit[0]: White pixel canceling enable
0x41	REG41	0x17	RW	Bit[7:6]: Reserved Bit[5]: UV_avg select 0: Median filter 1: Average filter Bit[4]: LENC gain adjust enable Bit[3]: SDE enable Bit[2]: UV_avg enable Bit[1]: CMX enable Bit[0]: CIP enable
0x42	REG42	0x00	RW	Bit[7:3]: Reserved Bit[2]: Read only latch select For indirect read: 0: vsync_rise 1: AWB_done Bit[1]: Average option for AEC 0: 5R+9G+2B 1: R+G+B Bit[0]: EOF select for AWB 0: pre_EOF 1: EOF_in
0x43	REG43	0x00	RW	Bit[7]: ISP test enable Bit[6]: ISP test Rolling horizontal bar enable Bit[5]: ISP test Test image + real image Bit[4]: ISP test ISP input data low bits = 0 Bit[3:2]: Color style 00: Normal bar 01: Vertical change bar 10: Horizontal change bar 11: Vertical change bar 2 Bit[1:0]: ISP test select 00: Bar 01: Random data 10: Squares 11: Black

table 7-1 system control registers (sheet 11 of 21)

address	register name	default value	RW	description
0x44	REG44	0x10	RW	Bit[7:6]: Reserved Bit[5]: ISP test, square 0: Color square 1: BW square Bit[4]: ISP test Random image reset enable (every frame is same) Bit[3:0]: ISP test Random image seed
0x45	INTERNAL CTRL	–	–	Internal Control Register
0x46	REG46	0x04	RW	Bit[7:0]: BLC target manual value
0x47	REG47	0x3F	RW	Bit[7]: bias_man_en Bit[6]: Reserved Bit[5]: LENC_bias_plus Bit[4]: LENC_bias_on Bit[3]: GMA_bias_plus Bit[2]: GMA_bias_on Bit[1]: LCD_bias_plus Bit[0]: LCD_bias_on
0x48~ 0x4B	DEBUG CTRL	–	–	Debug Control Registers
0x4C	REG4C	0x03	RW	Bit[7:3]: Reserved Bit[2:0]: R_X0[10:8]
0x4D	REG4D	0x30	RW	Bit[7:0]: R_X0[7:0]
0x4E	REG4E	0x02	RW	Bit[7:3]: Reserved Bit[2:0]: R_Y0[10:8]
0x4F	REG4F	0x5C	RW	Bit[7:0]: R_Y0[7:0]
0x50	REG50	0x00	RW	Bit[7]: Reserved Bit[6:0]: R_A1
0x51	REG51	0x00	RW	Bit[7:0]: R_B1
0x52	REG52	0xFF	RW	Bit[7:4]: R_B2 Bit[3:0]: R_A2
0x53	REG53	0x03	RW	Bit[7:3]: Reserved Bit[2:0]: G_X0[10:8]
0x54	REG54	0x30	RW	Bit[7:0]: G_X0[7:0]
0x55	REG55	0x02	RW	Bit[7:3]: Reserved Bit[2:0]: G_Y0[10:8]
0x56	REG56	0x5C	RW	Bit[7:0]: G_Y0[7:0]

table 7-1 system control registers (sheet 12 of 21)

address	register name	default value	RW	description
0x57	REG57	0x00	RW	Bit[7]: Reserved Bit[6:0]: G_A1
0x58	REG58	0x00	RW	Bit[7:0]: G_B1
0x59	REG59	0xFF	RW	Bit[7:4]: G_B2 Bit[3:0]: G_A2
0x5A	REG5A	0x03	RW	Bit[7:3]: Reserved Bit[2:0]: B_X0[10:8]
0x5B	REG5B	0x30	RW	Bit[7:0]: B_X0[7:0]
0x5C	REG5C	0x02	RW	Bit[7:3]: Reserved Bit[2:0]: B_Y0[10:8]
0x5D	REG5D	0x5C	RW	Bit[7:0]: B_Y0[7:0]
0x5E	REG5E	0x00	RW	Bit[7]: Reserved Bit[6:0]: B_A1
0x5F	REG5F	0x00	RW	Bit[7:0]: B_B1
0x60	REG60	0xFF	RW	Bit[7:4]: B_B2 Bit[3:0]: B_A2
0x61	REG61	0x0C	RW	Bit[7:5]: Reserved Bit[4:0]: Gain high threshold
0x62	REG62	0x06	RW	Bit[7]: Gain coefficient manual mode enable Bit[6:5]: Reserved Bit[4:0]: Gain low threshold
0x63	REG63	0x80	RW	Bit[7:0]: Coefficient threshold
0x64	REG64	0x80	RW	Bit[7:0]: Coefficient manual value
0x65	REG65	0x05	RW	Bit[7:0]: YST1
0x66	REG66	0x0C	RW	Bit[7:0]: YST2
0x67	REG67	0x1C	RW	Bit[7:0]: YST3
0x68	REG68	0x2A	RW	Bit[7:0]: YST4
0x69	REG69	0x29	RW	Bit[7:0]: YST5
0x6A	REG6A	0x45	RW	Bit[7:0]: YST6
0x6B	REG6B	0x52	RW	Bit[7:0]: YST7
0x6C	REG6C	0x5D	RW	Bit[7:0]: YST8
0x6D	REG6D	0x68	RW	Bit[7:0]: YST9
0x6E	REG6E	0x7F	RW	Bit[7:0]: YST10

table 7-1 system control registers (sheet 13 of 21)

address	register name	default value	RW	description
0x6F	REG6F	0x91	RW	Bit[7:0]: YST11
0x70	REG7	0xA5	RW	Bit[7:0]: YST12
0x71	REG71	0xC6	RW	Bit[7:0]: YST13
0x72	REG72	0xDE	RW	Bit[7:0]: YST14
0x73	REG73	0xEF	RW	Bit[7:0]: YST15
0x74	REG74	0x16	RW	Bit[7:0]: YSLP
0x75	REG75	0x5C	RW	Bit[7:6]: step_fast Bit[5:4]: step_local Bit[3]: g_en Bit[2]: AWB_SIMPLE Bit[1:0]: Advanced AWB control
0x76	REG76	0x00	RW	Bit[7:4]: max_fast_cnt Bit[3:0]: max_local_cnt
0x77	REG77	0x92	RW	Bit[7]: fast_enable Bit[6:4]: count_limit_ctrl Bit[3:0]: stable_range
0x78	REG78	0x21	RW	Bit[7:6]: count_area_sel Bit[5]: AWB_sim_sel 0: AWB 1: Gamma Bit[4]: AWB_RBlue Bit[3:0]: Advanced AWB control
0x79	REG79	0xE0	RW	Bit[7]: AWB_simF For AWB simple mode Bit[6]: awb_bias_plus For AWB_gain Bit[5]: AWB_bias_on For AWB_gain Bit[4]: AWB_bias_stat Bit[3]: AWB_freeze Bit[2]: AWB_preset Bit[1:0]: AWB_win
0x7A	REG7A	0x02	RW	Bit[7:0]: local_limit
0x7B	REG7B	0xFF	RW	Bit[7:0]: AWB_B_block
0x7C~ 0x88	AWB CTRL	–	–	Advanced AWB Control Registers
0x89	REG89	0xF0	RW	Bit[7:0]: red_limit
0x8A	REG8A	0xF0	RW	Bit[7:0]: green_limit
0x8B	REG8B	0xF0	RW	Bit[7:0]: blue_limit

table 7-1 system control registers (sheet 14 of 21)

address	register name	default value	RW	description
0x8C	REG8C	0x40	RW	Bit[7:0]: lcd_r_coef
0x8D	REG8D	0x40	RW	Bit[7:0]: lcd_g_coef
0x8E	REG8E	0x40	RW	Bit[7:0]: lcd_b_coef
0x8F	REG8F	0x1C	RW	Bit[7:5]: Reserved Bit[4:0]: Debug control Changing these registers is not recommended
0x90~ 0x9A	MANUAL CTRL	–	–	Manual Control (for debug purposes)
0x9B	REG9B	0x55	RW	Bit[7:6]: wt00 Bit[5:4]: wt01 Bit[3:2]: wt02 Bit[1:0]: wt03
0x9C	REG9C	0x55	RW	Bit[7:6]: wt10 Bit[5:4]: wt11 Bit[3:2]: wt12 Bit[1:0]: wt13
0x9D	REG9D	0x55	RW	Bit[7:6]: wt20 Bit[5:4]: wt21 Bit[3:2]: wt22 Bit[1:0]: wt23
0x9E	REG9E	0x55	RW	Bit[7:6]: wt30 Bit[5:4]: wt31 Bit[3:2]: wt32 Bit[1:0]: wt33
0x9F	REG9F	0x08	RW	Bit[7:0]: sharpenmt_t1
0xA0	REGA0	0x48	RW	Bit[7:0]: sharpenmt_t2
0xA1	REGA1	0x18	RW	Bit[7]: Reserved Bit[6:0]: sharpenmt_offset1 / manual sharpen threshold
0xA2	REGA2	0x0E	RW	Bit[7]: Reserved Bit[6:0]: sharpenmt_offset2
0xA3	REGA3	0x08	RW	Bit[7:0]: dns_t1
0xA4	REGA4	0x48	RW	Bit[7:0]: dns_t2
0xA5	REGA5	0x09	RW	Bit[7]: Reserved Bit[6:0]: dns_offset1 / manual DNS threshold
0xA6	REGA6	0x16	RW	Bit[7]: Reserved Bit[6:0]: dns_offset2
0xA7	REGA7	0x08	RW	Bit[7:0]: sharpenth_t1
0xA8	REGA8	0x48	RW	Bit[7:0]: sharpenth_t2

table 7-1 system control registers (sheet 15 of 21)

address	register name	default value	RW	description
0xA9	REGA9	0x04	RW	Bit[7]: cip_edge_mt_man_en Bit[6]: cip_bd_en Bit[5]: cip_dns_man_en Bit[4:0]: sharpenth_offset1 / manual sharpen TH threshold
0xAA	REGAA	0xA6	RW	Bit[7:5]: thre_rb_sharpen Bit[4:0]: sharpenth_offset2
0xAB	REGAB	0x33	RW	Bit[7:0]: CMX1
0xAC	REGAC	0x41	RW	Bit[7:0]: CMX2
0xAD	REGAD	0x0F	RW	Bit[7:0]: CMX3
0xAE	REGAE	0x0B	RW	Bit[7:0]: CMX4
0xAF	REGAF	0x44	RW	Bit[7:0]: CMX5
0xB0	REGB0	0x50	RW	Bit[7:0]: CMX6
0xB1	REGB1	0x55	RW	Bit[7:0]: CMX7
0xB2	REGB2	0x3A	RW	Bit[7:0]: CMX8
0xB3	REGB3	0x1C	RW	Bit[7:0]: CMX9
0xB4	REGB4	0x98	RW	Bit[7:0]: CMX_sign[7:0] Sign bits for CMX1 to CMX8
0xB5	REGB5	0x21	RW	Bit[7:6]: Reserved Bit[5]: UV_adjust TH2[8] (LSBs are at register 0xC0[7:0]) Bit[4]: ADJ_man_i Bit[3]: Y_avg_man Bit[2]: gamma_man Bit[1]: CMX_double Bit[0]: CMX_sign[8] Sign bit for CMX9
0xB6	REGB6	0x00	RW	SDE_Ctrl[7:0] Bit[7]: Fixed_Y_en Bit[6]: Negative_en Bit[5]: Gray_en Bit[4]: Fixed_U_en Bit[3]: Fixed_V_en Bit[2]: Y_contrast_en Bit[1]: Saturate_en Bit[0]: Hue_en
0xB7	REGB7	0x80	RW	Bit[7:0] Hue_cos
0xB8	REGB8	0x00	RW	Bit[7:0] Hue_sin

table 7-1 system control registers (sheet 16 of 21)

address	register name	default value	RW	description
0xB9	REGB9	0x40	RW	Bit[7:0]: Adjust value1 / manual saturate U / fixed U value
0xBA	REGBA	0x00	RW	Bit[7:0]: Adjust value2 / manually saturate V / fixed V value
0xBB	REGBB	0x00	RW	Bit[7:0]: Manual Y offset
0xBC	REGBC	0x20	RW	Bit[7:0]: Y contrast gain (20 = 1x)
0xBD	REGBD	0x00	RW	Bit[7:0]: YBRIGHTNESS
0xBE	REGBE	0x01	RW	Bit[7:6]: Reserved Bit[5:0]: SGNSET[5:0] SGN0=1, SGN1=0, SGN4=SGN5=0: Hue SGN0=0, SGN1=1, SGN4=SGN5=0: Hue SGN0=1, SGN1=0, SGN4=SGN5=1: Hue SGN0=0, SGN1=1, SGN4=SGN5=1: Hue SGN2: YOFFSET SGN3: YBRIGHTNESS
0xBF	REGBF	0x10	RW	Bit[7:0]: UV_adjust TH1
0xC0	REGC0	0x00	RW	Bit[7:0]: UV_adjust TH2[7:0] (MSB is at register 0xB5[5])
0xC1	DVP_CTRL00	0x00	RW	DVP Control 00 Bit[7:6]: Reserved for debug only Bit[5]: data_10_3F0 0: No limit 1: Limit data between 0x10 and 0x3F0 in CC656 Bit[4]: data_40_3C0 0: No limit 1: Limit data between 0x40 and 0x3C0 in CC656 Bit[3]: DBG_OUT 0: Normal 1: Debug mode Bit[2]: BT_BIT8 0: Bit test pattern uses 10-bit data 1: Bit test pattern uses 8-bit data Bit[1]: BT_M1 0: Bit test pattern shifts one bit in every clock period 1: Bit test pattern shifts one bit in every two clock periods Bit[0]: BT_OUT 0: Output normal image 1: Output bit test pattern

table 7-1 system control registers (sheet 17 of 21)

address	register name	default value	RW	description
0xC2	DVP_CTRL01	0x00	RW	DVP Control 01 Bit[7:6]: DATA_ORDER 00: DVP output DVP_DATA[9:0] 01: DVP output DVP_DATA[0:9] 10: DVP output DVP_DATA{[2:9], [1:0]} 11: DVP output DVP_DATA{[7:0], [9:8]} Bit[5]: D_POL 0: Normal 1: Output bit is reversed Bit[4]: HREF_POL 0: Normal 1: HREF will be reversed Bit[3]: VSYNC_POL 0: Normal 1: VSYNC will be reversed Bit[2]: PCLK_POL 0: Normal 1: PCLK will be reversed Bit[1:0]: Reserved
0xC3	IO	0x00	RW	Bit[7:6]: pad Adjust drive capability of IO pad Bit[5]: dselreg 0: GPIO[1:0] select image data least significant 2 bits 1: GPIO[1:0] select register value from DVP2[1:0] (0x0D) at output Bit[4]: Output enable of HREF pin 0: Input 1: Output Bit[3]: Output enable of VSYNC pin 0: Input 1: Output Bit[2]: Output enable of PCLK pin 0: Input 1: Output Bit[1:0]: Output enable of DATA[9:8] pin 0: Input 1: Output
0xC4	IO	0x00	RW	Bit[7:0]: Output enable for DATA[7:0] pin 0: Input 1: Output
0xC5	SHIFT	0x90	RW	Bit[7:0]: Offset of data shift start point
0xC6	SA1TMC0	0x30	RW	Bit[7:6]: yend Adjust rstyz start point Bit[5:0]: Reserved
0xC7~ 0xCC	SENSOR TIMING CTRL	–	–	Timing Control Registers

table 7-1 system control registers (sheet 18 of 21)

address	register name	default value	RW	description
0xCD	SA1TMC7	0x12	RW	Bit[7]: cbar 0: Normal image 1: Enable sensor color bar Bit[6]: wtest 0: Normal 1: White image in color bar mode Bit[5:0]: Reserved
0xCE	REGCE	0x00	RW	Indirect Register Read Address
0xCF	REGCF	–	R	Indirect Register Read Data
0xD0~ 0xD8	SENSOR ANALOG CTRL	–	–	Analog Control Registers
0xD9	ANCOM1	0x01	RW	Bit[7:6]: pgain[1:0] Bit[5:0]: Reserved
0xDA	PWCOM0	0x07	RW	Bit[7]: bp_regulator Bit[6:0]: Reserved
0xDB	SENSOR ANALOG CTRL	–	–	Analog Control Registers
0xDC	PWCOM2	0x27	RW	Bit[7:4]: Reserved Bit[3:0]: vsun_c[3:0]
0xDD	SENSOR ANALOG CTRL	–	–	Analog Control Registers
0xDE	PWCOM4	0xC4	RW	Bit[7:4]: Reserved Bit[3]: tagc (ana) 0: Pre-gain in AGC loop, pg[1:0] = {AGC[4], AGC[4]} 1: Pre-gain manually control, pg[1:0] = register 0xD9[7:6] Bit[2:0]: Reserved
0xDF	GRPC	0x10	RW	Bit[7]: grpw_en 0: SCCB group write is disabled or has been finished 1: Enable SCCB group write function Bit[6:5]: Reserved Bit[4:0]: grpw_bct Byte counts of data need to be updated at current group write
0xE0	GADD1	0x00	RW	Bit[7:0]: grpw_add1 First register address for SCCB group write
0xE1	GDAT1	0x00	RW	Bit[7:0]: grpw_dat1 First data for SCCB group write, this data will be written into register which address is specified in grpw_add1

table 7-1 system control registers (sheet 19 of 21)

address	register name	default value	RW	description
0xE2	GADD2	0x00	RW	Bit[7:0]: grpw_add1 Second register address for SCCB group write
0xE3	GDAT2	0x00	RW	Bit[7:0]: grpw_dat2 Second data for SCCB group write, this data will be written into register which address is specified in grpw_add2
0xE4	GADD3	0x00	RW	Bit[7:0]: grpw_add3 Third register address for SCCB group write
0xE5	GDAT3	0x00	RW	Bit[7:0]: grpw_dat3 Third data for SCCB group write, this data will be written into register which address is specified in grpw_add3
0xE6	GADD4	0x00	RW	Bit[7:0]: grpw_add4 Fourth register address for SCCB group write
0xE7	GDAT4	0x00	RW	Bit[7:0]: grpw_dat4 Fourth data for SCCB group write, this data will be written into register which address is specified in grpw_add4
0xE8	GADD5	0x00	RW	Bit[7:0]: grpw_add5 Fifth register address for SCCB group write
0xE9	GDAT5	0x00	RW	Bit[7:0]: grpw_dat5 Fifth data for SCCB group write, this data will be written into register which address is specified in grpw_add5
0xEA	GADD6	0x00	RW	Bit[7:0]: grpw_add6 Sixth register address for SCCB group write
0xEB	GDAT6	0x00	RW	Bit[7:0]: grpw_dat6 Sixth data for SCCB group write, this data will be written into register which address is specified in grpw_add6
0xEC	GADD7	0x00	RW	Bit[7:0]: grpw_add7 Seventh register address for SCCB group write
0xED	GDAT7	0x00	RW	Bit[7:0]: grpw_dat7 Seventh data for SCCB group write, this data will be written into register which address is specified in grpw_add7
0xEE	GADD8	0x00	RW	Bit[7:0]: grpw_add8 Eighth register address for SCCB group write

table 7-1 system control registers (sheet 20 of 21)

address	register name	default value	RW	description
0xEF	GDAT8	0x00	RW	Bit[7:0]: grpw_dat8 Eighth data for SCCB group write, this data will be written into register which address is specified in grpw_add8
0xF0	GADD9	0x00	RW	Bit[7:0]: grpw_add9 Ninth register address for SCCB group write
0xF1	GDAT9	0x00	RW	Bit[7:0]: grpw_dat9 Ninth data for SCCB group write, this data will be written into register which address is specified in grpw_add9
0xF2	GADD10	0x00	RW	Bit[7:0]: grpw_add10 Tenth register address for SCCB group write
0xF3	GDAT10	0x00	RW	Bit[7:0]: grpw_dat10 Tenth data for SCCB group write, this data will be written into register which address is specified in grpw_add10
0xF4	GADD11	0x00	RW	Bit[7:0]: grpw_add11 Eleventh register address for SCCB group write
0xF5	GDAT11	0x00	RW	Bit[7:0]: grpw_dat11 Eleventh data for SCCB group write, this data will be written into register which address is specified in grpw_add11
0xF6	GADD12	0x00	RW	Bit[7:0]: grpw_add12 Twelfth register address for SCCB group write
0xF7	GDAT12	0x00	RW	Bit[7:0]: grpw_dat12 Twelfth data for SCCB group write, this data will be written into register which address is specified in grpw_add12
0xF8	GADD13	0x00	RW	Bit[7:0]: grpw_add13 Thirteenth register address for SCCB group write
0xF9	GDAT13	0x00	RW	Bit[7:0]: grpw_dat13 Thirteenth data for SCCB group write, this data will be written into register which address is specified in grpw_add13
0xFA	GADD14	0x00	RW	Bit[7:0]: grpw_add14 Fourteenth register address for SCCB group write
0xFB	GDAT14	0x00	RW	Bit[7:0]: grpw_dat14 Fourteenth data for SCCB group write, this data will be written into register which address is specified in grpw_add14

table 7-1 system control registers (sheet 21 of 21)

address	register name	default value	RW	description
0xFC	GADD15	0x00	RW	Bit[7:0]: grpw_add15 Fifteenth register address for SCCB group write
0xFD	GDAT15	0x00	RW	Bit[7:0]: grpw_dat15 Fifteenth data for SCCB group write, this data will be written into register which address is specified in grpw_add15
0xFE	GADD16	0x00	RW	Bit[7:0]: grpw_add16 Sixteenth register address for SCCB group write
0xFF	GDAT16	0x00	RW	Bit[7:0]: grpw_dat16 Sixteenth data for SCCB group write, this data will be written into register which address is specified in grpw_add16

8 operating specifications

8.1 absolute maximum ratings

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +95°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-D}	3V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

8.2 functional temperature

table 8-2 functional temperature

parameter	range
operating temperature range[a]	-20°C to +70°C
stable operating temperature range[b]	0°C to +50°C

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

8.3 DC characteristics

table 8-3 DC characteristics (T_A = 23°C ± 2°C)

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	2.6	2.8	3.0	V
V_{DD-D}[a]	supply voltage (digital core)	1.425	1.5	1.575	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	3.0	V
I_{DD-A}	active (operating) current		35	45	mA
I_{DD-IO}[b]			32	50	mA
$I_{DDS-SCCB}$	standby current		0.08	0.12	mA
$I_{DDS-PWDN}$			30	75	µA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.5V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[c]	SIO_C and SIO_D	-0.5	0	0.54	V
V_{IH}[c]	SIO_C and SIO_D	1.26	1.8	2.3	V

a. using the internal regulator is strongly recommended for minimum power down currents

b. active current is based on sensor resolution at full size and full speed, with the MIPI function, the active current needs an additional 20mA.

c. based on DOVDD = 1.8V.

8.4 AC characteristics

table 8-4 AC characteristics (T_A = 25°C, V_{DD-A} = 2.8V)

symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth		30		MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	settling time for hardware reset			<1	ms
	settling time for software reset			<1	ms
	settling time for resolution mode change			<1	ms
	settling time for register setting			<300	ms

8.5 timing characteristics

table 8-5 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK)	6	24	27(54[a])	MHz
t_r, t_f	clock input rise/fall time			5 (10[b])	ns

a. if using the internal clock pre-scaler

b. if using the internal PLL

figure 8-1 SCCB interface timing

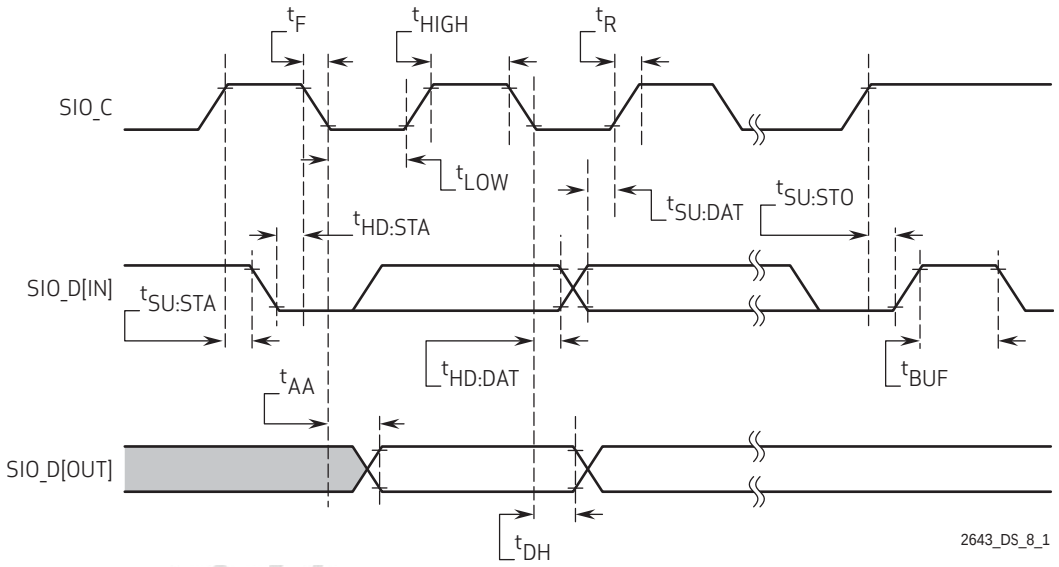


table 8-6 SCCB interface timing specifications[ab]

symbol	parameter	min	typ	max	unit
f_{SIO_C}	clock frequency			400	KHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	0.6			µs
t_{AA}	SIO_C low to data out valid	0.1		0.9	µs
t_{BUF}	bus free time before new start	1.3			µs
$t_{HD:STA}$	start condition hold time	0.6			µs
$t_{SU:STA}$	start condition setup time	0.6			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.1			µs
$t_{SU:STO}$	stop condition setup time	0.6			µs
t_R, t_F	SCCB rise/fall times			0.3	µs
t_{DH}	data out hold time	0.05			µs

a. SCCB timing is based on 400KHz mode

b. timing measurement shown at the beginning of the rising edge or/and of the falling edge signifies 10%, timing measurement shown in the middle of the rising/falling edge signifies 50%, timing measurement shown at the beginning of the rising edge or/and of the falling edge signifies 90%

figure 8-2 line/pixel output timing

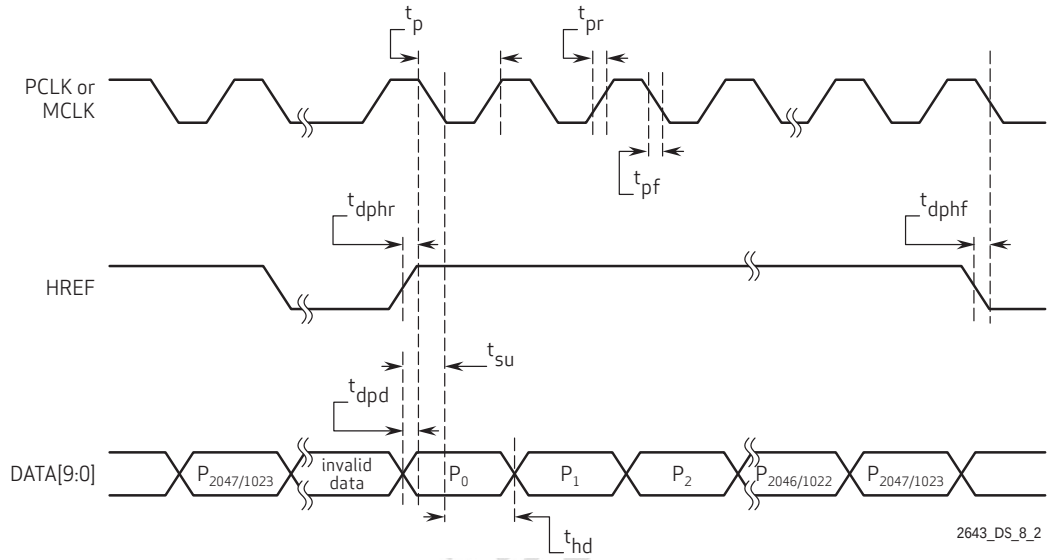


table 8-7 pixel timing specifications[a]

symbol	parameter	min	typ	max	unit
t_p	PCLK period[b]		13.89		ns
t_{pr}	PCLK rising time[b]		2.1		ns
t_{pf}	PCLK falling time[b]		1.1		ns
t_{dphr}	PCLK negative edge to HREF rising edge		1.2		ns
t_{dphf}	PCLK negative edge to HREF negative edge		0.5		ns
t_{dpd}	PCLK negative edge to data output delay	0		3	ns
t_{su}	data bus setup time	7.0	9.0		ns
t_{hd}	data bus hold time	3.6	4.3		ns

a. timing measurement shown at the beginning of the rising edge or/and of the falling edge signifies 10%, timing measurement shown in the middle of the rising/falling edge signifies 50%, timing measurement shown at the beginning of the rising edge or/and of the falling edge signifies 90%

b. PCLK running at 72 MHz, C_L = 10pF, and DOVDD = 2.8V

9 mechanical specifications

9.1 physical specifications

figure 9-1 package specifications

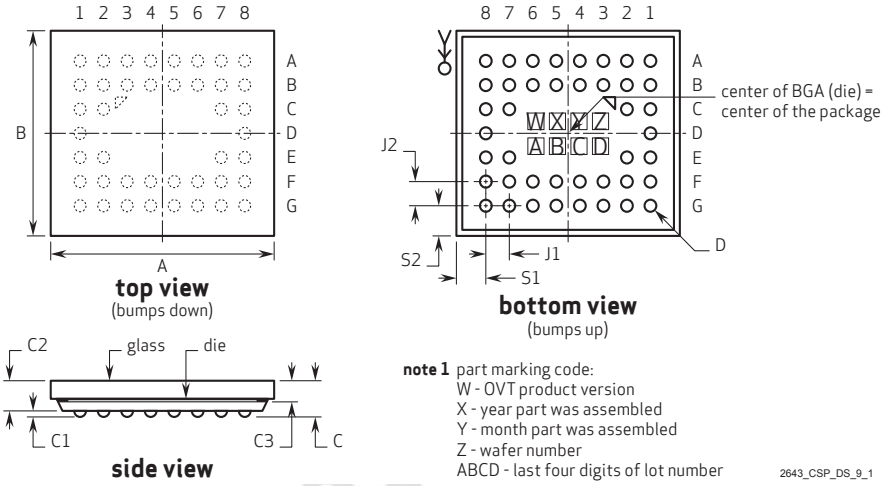


table 9-1 package dimensions

parameter	symbol	min	typ	max	unit
package body dimension x	A	5010	5035	5060	µm
package body dimension y	B	4610	4635	4660	µm
package height	C	720	780	840	µm
ball height	C1	130	160	190	µm
package body thickness	C2	575	620	665	µm
thickness of glass surface to wafer	C3	425	445	465	µm
ball diameter	D	270	300	330	µm
total pin count	N		42 (12 NC)		
pin count x-axis	N1		8		
pin count y-axis	N2		7		
pins pitch x-axis	J1		600		µm
pins pitch y-axis	J2		620		µm
edge-to-pin center distance analog x	S1	388	418	448	µm
edge-to-pin center distance analog y	S2	428	458	488	µm

9.2 IR reflow specifications

note
The OV2643 uses a lead free package.

figure 9-2 IR reflow ramp rate requirements

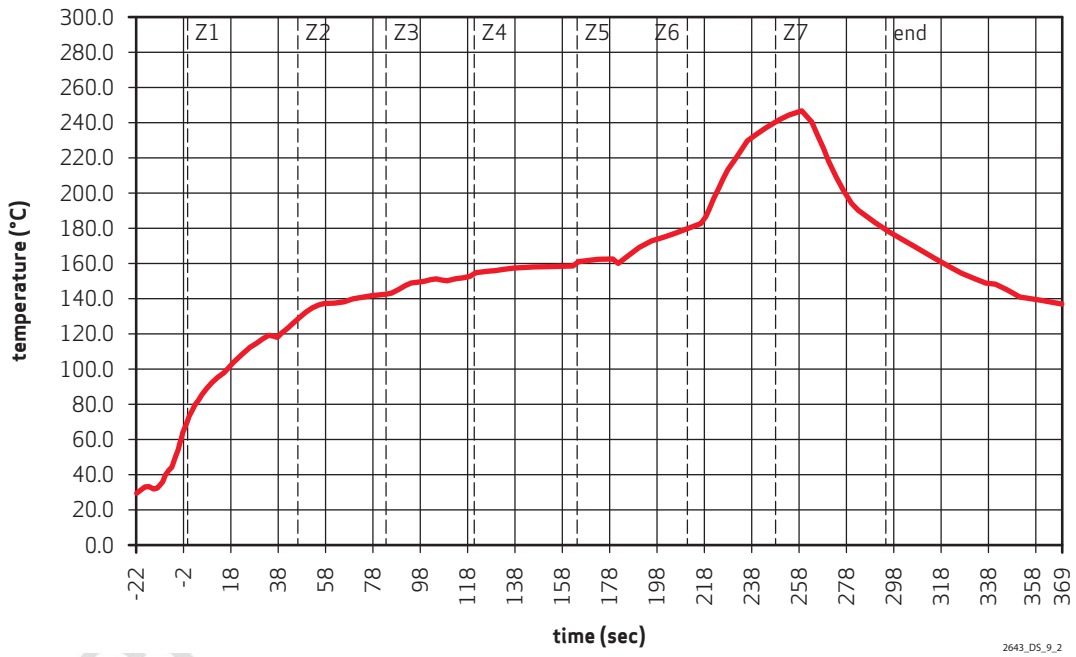


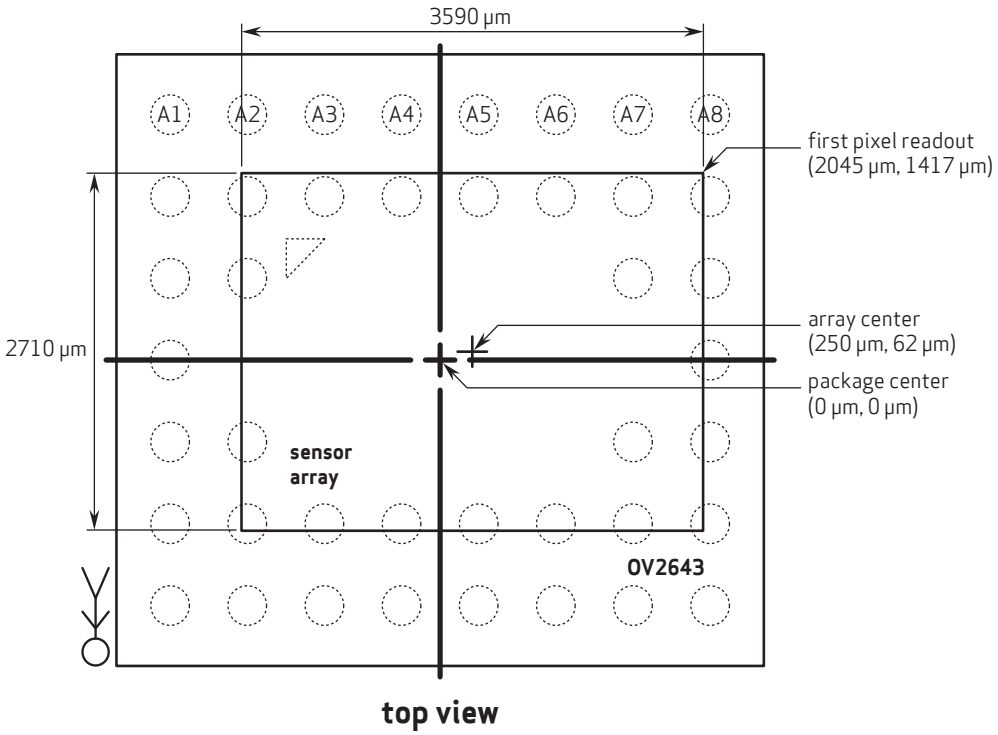
table 9-2 reflow conditions

condition	exposure
average ramp-up rate (30°C to 217°C)	less than 3°C per second
> 100°C	between 330 - 600 seconds
> 150°C	at least 210 seconds
> 217°C	at least 30 seconds (30 ~ 120 seconds)
peak temperature	245°C
cool-down rate (peak to 50°C)	less than 6°C per second
time from 30°C to 245°C	no greater than 390 seconds

10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pin A1 to A8 oriented down on the PCB.

2643_CSP_DS_10_1

10.2 lens chief ray angle (CRA)

figure 10-2 chief ray angle (CRA)

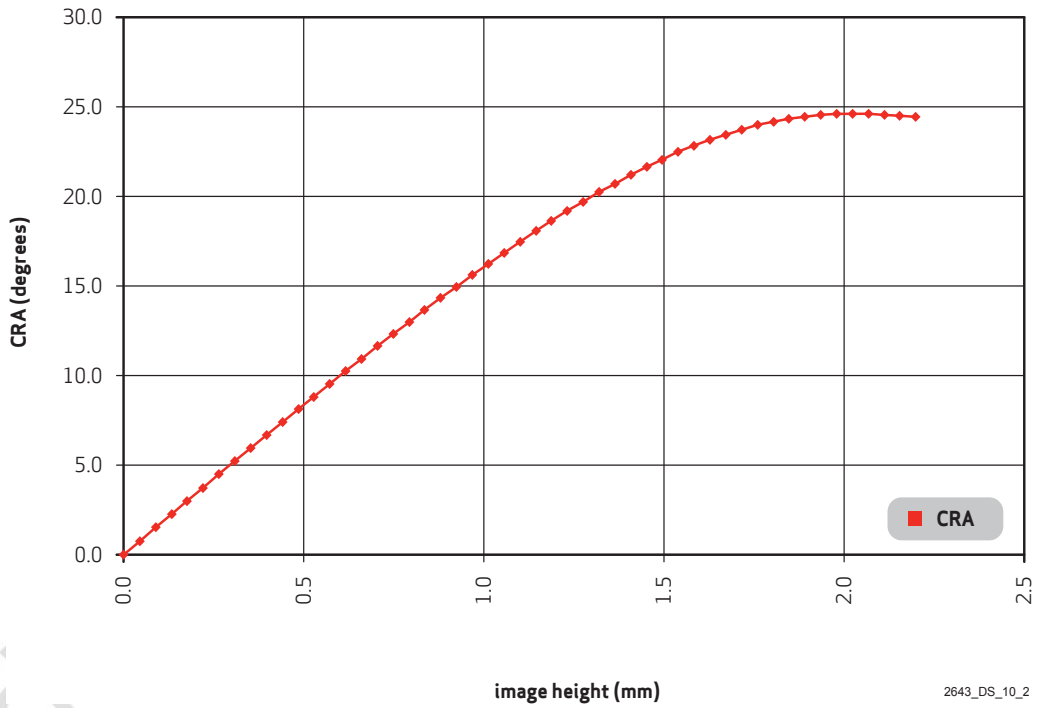


table 10-1 CRA versus image height plot (sheet 1 of 3)

field (%)	image height (mm)	CRA (degrees)
0	0	0
0.02	0.044	0.7455
0.04	0.088	1.4905
0.06	0.132	2.2343
0.08	0.176	2.9766
0.1	0.22	3.7168
0.12	0.264	4.4544
0.14	0.308	5.1892
0.16	0.352	5.9206
0.18	0.396	6.6484

table 10-1 CRA versus image height plot (sheet 2 of 3)

field (%)	image height (mm)	CRA (degrees)
0.2	0.44	7.3723
0.22	0.484	8.0919
0.24	0.528	8.807
0.26	0.572	9.5172
0.28	0.616	10.2221
0.3	0.66	10.9214
0.32	0.704	11.6146
0.34	0.748	12.3011
0.36	0.792	12.9804
0.38	0.836	13.6517
0.4	0.88	14.3143
0.42	0.924	14.9673
0.44	0.968	15.6099
0.46	1.012	16.241
0.48	1.056	16.8595
0.5	1.1	17.4643
0.52	1.144	18.0543
0.54	1.188	18.628
0.56	1.232	19.1843
0.58	1.276	19.7218
0.6	1.32	20.239
0.62	1.364	20.7347
0.64	1.408	21.2073
0.66	1.452	21.6554
0.68	1.496	22.0776
0.7	1.54	22.4725
0.72	1.584	22.8385
0.74	1.628	23.1743
0.76	1.672	23.4785
0.78	1.716	23.7497

table 10-1 CRA versus image height plot (sheet 3 of 3)

field (%)	image height (mm)	CRA (degrees)
0.8	1.76	23.9866
0.82	1.804	24.1881
0.84	1.848	24.3532
0.86	1.892	24.4813
0.88	1.936	24.5722
0.9	1.98	24.6267
0.92	2.024	24.646
0.94	2.068	24.6328
0.96	2.112	24.5913
0.98	2.156	24.5268
1	2.2	24.4459

revision history

version 1.0 11.02.2009

- initial release

version 2.0 08.18.2010

- in the key specifications section, updated all TBD values
- in chapter 6, updated table 6-2 DVP timing specification SVGA timing value from:

(1) 1200000 tp
(2) 3000 tp
(3) 283910 tp
(4) 1500 tp
(5) 13090 tp
(6) 800 tp
(7) 700 tp

changed to

(1) 799500 tp
(2) 2460 tp
(3) 48110 tp
(4) 1230 tp
(5) 13090 tp
(6) 800 tp
(7) 430 tp

- in chapter 8, updated table 8-3 DC characteristics by replacing all TBD values

the clear advantage™

OmniVision Technologies, Inc.

UNITED STATES

4275 Burton Drive
Santa Clara, CA 95054

tel: + 1 408 567 3000

fax: + 1 408 567 3001

email: salesamerican@ovt.com

UNITED KINGDOM

Hampshire + 44 1256 744 610

FINLAND

Mouhijärvi + 358 3 341 1898

GERMANY

Munich +49 89 63 81 99 88

CHINA

Beijing + 86 10 6580 1690

Shanghai + 86 21 6105 5100

Shenzhen + 86 755 8384 9733

Hong Kong + 852 2403 4011

JAPAN

Tokyo + 81 3 5765 6321

KOREA

Seoul + 82 2 3478 2812

SINGAPORE + 65 6562 8250

TAIWAN

Taipei + 886 2 2657 9800 - ext.#100

website: **www.ovt.com**